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Gravity Probe B Relativity Mission

GPB GSS ACU CLOCK FREQUENCY TEST

GP-B Procedure P0959 Rev -

DUT PN: 26225-101 REV _____ SN: _____

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FSU Test RE, Gyroscope Suspension System (GSS) Group

Date

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Date

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GP-B Quality Assurance

Date

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Date

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1.0 Revision History

Rev Level	Comments/notes	Date	Revised By
-	First release of this test procedure	12-Nov-2002	J. Dusenbury

2.0 Scope:

This procedure details the operations required to perform a box-level functional test of the clock circuitry in the GSS Aft Control Unit (ACU), PN 26226-101 to verify requirement 3.2.8.7 of GSS Spec PLSE-13-1A which requires that “The frequency of the GSS internal backup 16fo clock shall be 16.368000 MHz, +/- 1500 Hz (+/- 91 ppm)”

The test methodology is to connect a EU FSU box to a Flight ACU and spacecraft emulator, and measure the 16fo/15 clock on the FSU Forward Comm Link (FCL) board, and multiplying the result by 15 to obtain the ACU clock frequency. Where applicable, an external clock will be provided from an external function generator to the Spacecraft Emulator (See Figure 1).

Two tests will be run:

- 1) The system will be operated in normal configuration with the ACU clock locked to the external function generator. The PLL-locked condition will be verified by observing the function generator and derived clock on an oscilloscope. Engineering data will be taken while the function generator frequency is varied to determine the lock range of the ACU clock
- 2) The ACU will then be operated without the timing signal from the Spacecraft Emulator, and the free running frequency of the ACU clock will be measured on the frequency counter as before.

Requirement 3.2.8.7 will be met when:

- The locked frequency is within 1500 Hz of 16.368 MHz when the function generator frequency is nominal, and
- The unlocked frequency is within 1500 Hz of 16.368 MHz when the spacecraft emulator clock is disabled

3.0 Device Under Test (DUT):

Record the serial number of the Device Undergoing Test, or DUT.

26226-101 GSS Aft Suspension Unit (FSU)	SN:	
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Test Operator:	Name:	
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Start of test:	Date: Time:	
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4.0 Formal Requirements Verification

This procedure verifies by test the following requirements GSS Requirements:

Requirement 3.2.8.7 of GSS Spec PLSE-13-1A which requires that "The frequency of the GSS internal backup 16fo clock shall be 16.368000 MHz, +/- 1500 Hz (+/- 91 ppm)"

5.0 Reference Documents

- 5.1 PLSE 13-1 Rev A GSS Specification
- 5.2 26226 Assembly Drawing for the Aft Suspension Unit (ASU)
- 5.3 S0477 Rev A GSS Interface Control Document (ICD)
- 5.4 MIL-STD-1686 Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment

6.0 Test Facilities

- 6.1 Primary facility: End Station 3 : Main Lab (HEPL 175), Stanford University

7.0 QA Provisions:

- 7.1 This procedure shall be conducted on a formal basis to its latest approved and released version. The QA Program Engineer (D. Ross) and the government representative (ONR/R. Gurr) shall be notified 24 hours prior to the start of this procedure. QA may monitor the execution of all or part of this procedure should they elect to do so.

QA notification time/date:

Date/time: _____
GP-B QA (D. Ross)

Date/time: _____
Gov't Rep (R. Gurr)

- 7.2 Upon completion of this procedure, the GSS manager and the GP-B QA manager shall certify her/his concurrence that the procedure was performed and accomplished in accordance with the prescribed instructions by signing and dating his approval at the end of this procedure.

8.0 Test Personnel

This test procedure is to be conducted only by the following personnel, or others designated by the GSS RE at the time of test (redline names in below as required)

- 8.1 Jay Dusenbury
8.2 Scott Smader
8.3 Other: _____

9.0 General Instructions

- 9.1 Redlines can be initiated by the test personnel listed in Section 8.0 and must be approved by QA.
- 9.2 Test operators shall read this procedure in its entirety and resolve any apparent ambiguities prior to beginning this test.
- 9.3 Any nonconformance or test anomaly should be reported by via a Discrepancy Log (D-LOG). Refer to the Quality Plan, P0108, for guidance. Do not alter or break test configuration if a test failure occurs; notify quality assurance.
- 9.4 Only the following persons have the authority to exit/terminate this test or perform a retest: test operators listed in Section 8.0 and GP-B QA.

10.0 Hardware Safety Requirements:

- 10.1 This assembly is ESD sensitive; special care shall be exercised per the "Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment", MIL-STD-1686
- 10.2 Ensure that power is removed from cable assemblies before connecting or disconnecting cable connectors.
- 10.3 Connector savers are to be used on all flight connector interfaces unless otherwise specified.
- 10.4 Connector mating:
- 10.4.1 Examine all mating connectors before attempting to mate them.
- 10.4.2 Remove any foreign particles. Look for any damaged pins or sockets.
- 10.4.3 Do not force the coupling action if excessive resistance is encountered.
- 10.4.4 Ensure that key-ways are aligned when mating connectors.

11.0 External Test Equipment

The following support hardware will be used and the applicable information for the instruments shall be recorded below. Hand-written additions to this list may be made in the space provided.

Item	Equipment Description	Qty	Make	PN	SN	Cal Due
1.	GSS Spacecraft emulator	1	SU	NA		
2.	2-stub 1553 coupler	2	MilesTek	90-50202	NA	NA
3.	GSS testset workstation	1	SU	NA	NA	NA
4.	GSE power cable	1	LMCO	8A02084GSE-101	NA	NA
5.	GSE timing cable	1	LMCO	8A02085GSE-101	NA	NA
6.	GSE GFAB A cable	1	LMCO	8A01473-101	NA	NA
7.	GSE GFAB B cable	1	LMCO	8A01474-101	NA	NA
8.	GSE 1553 cable	1	LMCO	8A00673GSE-501	NA	NA
9.	1553 terminator	2	MilesTek	10-06403-025	NA	NA
10.	1553 patch cable	2	Trompeter	CA-2014-120	NA	NA
11.	GSS ASU flight unit	1	SU	26226-101	NA	NA
12.	GSS APU/FSU power cable	1	LMCO	8A01471-101	NA	NA
13.	Oscilloscope	1				
14.	Function Generator	1				
15.	Frequency Counter					

12.0 Test Connection and Application of Power

Note: All handling of this DUT shall be performed using ESD control methods, as outlined in MIL-STD-1686. Unit shall be inspected at an ESD certified station. Wrist straps and/or heel grounding straps shall be used.

Important: Ensure that power is removed from cable assemblies before connecting or disconnecting cable connectors.

	P/F	Notes
12.1.1 Remove DUT from storage container. Verify that all connectors appear undamaged		
12.1.2 Verify all Aft power supplies are turned off on the Spacecraft Emulator panel.		
12.1.3 Connect FSU to ASU (DUT) and GSE as shown in Fig. 1.		
12.1.4 Set current limit on HP power supply in S/C emulator rack to 5.0 A <ul style="list-style-type: none"> • Close any LabView program that may be running. • Key in the following sequence on the front panel of the HP supply: • “LOCAL, Function: CURRENT, 5.0, ENTER” 		
12.1.5 Restart the LabView <i>GSE Test</i> virtual instrument.		
12.1.6 Set supply voltage to 28.0 V on the <i>GSE test</i> panel.		
12.1.7 Set Spacecraft clock emulator to the following: <p>16fo: A + B</p> <p>10 Hz: A + B</p> <p>Sun 10 Hz: A + B</p>		
12.1.8 Apply power to the aft box by turning on “Aft Main” on LabView control panel; record power on time in Power Log for this unit.		
12.1.9 Verify that current is < 550 mA; if greater remove power and cancel test.		
12.1.10 Record indicated main bus current as indicated on HP power supply front panel.		Current:
12.1.11 Record power-on start time in power log for the DUT and the power and operations log for the FU ASU.		
12.1.12 Apply power to the forward GSS by turning on the lab power supply		

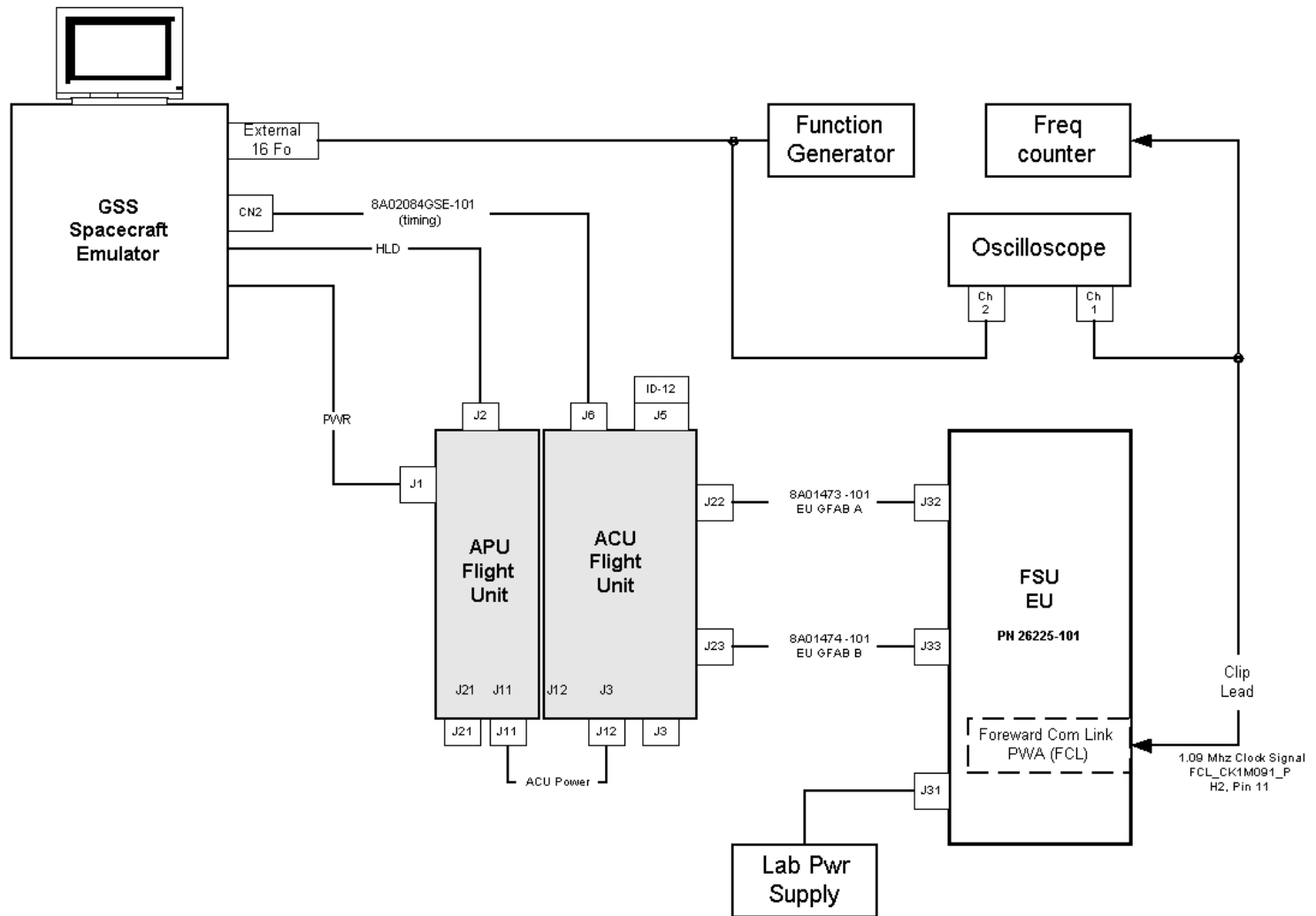


Figure 1 Clock Test Setup

13.0 ASU Clock Testing - Locked:

	P/F	Notes
13.1 Enable the function generator input to the spacecraft emulator by setting S1 on the emulator PC board to the "+5" position		
13.2 Set the function generator frequency to 16.368 MHz and the amplitude to TTL		
13.3 Observe the function generator input and the FCL_CK1M091_P signals on the oscilloscope. Trigger on the function generator input (Ch1) and adjust horizontal and vertical settings until both signals can be seen clearly		
13.4 Verify that a "locked" condition exists between the function generator input and the FCL_CK1 signal (both signals are stationary on the scope display).		
13.5 Lower the function generator setting in small increments until the FCL_CK1M091_P "unlocks" (signal will not be stationary on the scope).		
13.6 Record lowest "locked" frequency at right		Freq =
13.7 Raise the function generator setting in small increments until the FCL_CK1M091_P "unlocks" (signal will not be stationary on the scope).		
13.8 Record highest "locked" frequency at right		Freq =

14.0 ASU Clock Testing - Unlocked:

	P/F	Notes
14.1 Disconnect the 8A02084GSE-101 timing cable from the emulator CN2, leaving the other end connected to the DUT		
14.2 Record the "unlocked" frequency of the FCL_CK1M091_P signal		Freq =
14.3 Verify that the signal is 1091.2+/-100 Hz		

15.0 Completion of procedure:

	P/F	Notes
15.1 Remove power to both the forward and aft boxes.		
15.2 Return DUT to storage container if applicable.		

16.0 Certification:

I certify that this procedure was performed in whole and that the data recorded above is complete and accurate.

Test Engineer Date

This is to certify that the information obtained under this test procedure is as represented and the documentation is completed and correct.

GSS Representative Date

Quality Assurance Date