W. W. Hansen Experimental Physics Laboratory
STANFORD UNIVERSITY
STANFORD, CALIFORNIA 94305-4085

Gravity Probe B Relativity Mission

APU POST REWORK TEST PROCEDURE

GP-B Procedure
P0698 Rev A

DUT PN: BE02598032 REV - SN: _____

Date Performed:_____

Test Operator:_____

Test Phase/Note:_____

Prepared by: William Bencze Date
RE, Gyroscope Suspension System (GSS) Group

Approved by: William Bencze Date
Payload Electronics Manager.

Approved by: Dorrene Ross Date
GP-B Quality Assurance

Table of Contents:

1.0 Revision History

Rev Level	Comments/notes	Date	Revised By
-	First release of this test procedure	24-Jan-01	WJ Bencze
A	This revision was created to fix some errors.	1-Mar-2001	R Zilm

2.0 Scope:

This procedure details the operations required to perform a box-level electrical functional test on a Battel Engineering APU, PN BE02598032.

This is an abbreviated test and thus does not test all aspects of the APU; it is primarily designed to confirm that the APU primary voltage outputs are functional after

3.0 Formal Requirements Verification

This procedure does not verify any program level requirements

4.0 Reference Documents

4.1.	PLSE 13-1 Rev A	GSS Specification
4.2.	MIL-STD-1686	Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment

5.0 Test Facilities

5.1. Primary facility: NASA/Ames vibration test lab.

5.2. Alternate facility (specify):_____

6.0 QA Provisions:

6.1. This procedure shall be conducted on a formal basis to its latest approved and released version. The QA Program Engineer (D. Ross) and the Government representative (E. Ingraham) shall be notified 24 hours prior to he start of this procedure. QA may monitor the execution of all or part of this procedure should they elect to do so.

Date/time:_____	Date/time:_____
GP-B QA (D. Ross)	Government Rep. (E. Ingraham)

6.2. Upon completion of this procedure, the GSS manager and the GP-B QA manager shall certify her/his concurrence that the procedure was performed and accomplished in accordance with the prescribed instructions by signing and dating his approval at the end of this procedure.

7.0 Test Personnel

This test procedure is to be conducted only by the following personnel, or others designated by the GSS RE at the time of test (redline names in below as required)

7.1. William Bencze

7.2. Ron Zilm

7.3. Rick Bevan

7.4. Steve Battel (Battel Engineering)

7.5. James Tom (Battel Engineering)

7.6. Other: _____

8.0 General Instructions

8.1. Redlines can be initiated by the test personnel listed in Section 7.0 and must be approved by QA.

8.2. Test operators shall read this procedure in its entirety and resolve any apparent ambiguities prior to beginning this test.

8.3. Any nonconformance or test anomaly should be reported by a Discrepancy Report. Refer to the Quality Plan, P0108, for guidance. Do not alter or break test configuration if a test failure occurs; notify quality assurance.

8.4. Only the following persons have the authority to exit/terminate this test or perform a retest: test operators listed in Section 7.0 and GP-B QA.

9.0 Hardware Safety and Data Recording Requirements

9.1. Electrostatic Discharge (ESD) Protection:

9.1.1. This assembly is ESD sensitive; special care shall be exercised per the “Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment”, MIL-STD-1686.

9.2. Connectors/Cables:

9.2.1. Ensure that power is removed from cable assemblies before connecting or disconnecting cable connectors.

9.2.2. Connector savers are to be used on all flight connector interfaces unless otherwise specified.

9.2.3. All mates and de-mates to flight connector interfaces (not to connector saver interfaces) shall be recorded in the **Connector Mate/Demate Log** for this assembly

9.2.4. Connectors shall be examined before attempting to mate them. Remove any foreign particles. Look for any damaged pins or sockets. Do not force the coupling action if excessive resistance is encountered. Ensure that key-ways are aligned when mating connectors.

10.0 External Test Equipment

The following support hardware will be used and the applicable information for the instruments shall be recorded below. Hand-written additions to this list may be made in the space provided.

Item	Equipment Description	Qty	Make	PN	SN	Cal Due
1.	GSS Spacecraft emulator	1	SU	NA	01	
2.	Multimeter	1	Fluke			
3.	Multimeter	1	Fluke			
4.	Multimeter	1	Fluke			
5.	Multimeter	1	Fluke			
6.	Multimeter	1	Fluke			
7.	GSE Power cable	1	LMMS	8A02083GSE-101	NA	NA
8.	GSE Power cable	1	LMMS	8A02083GSE-102	NA	NA
9.	APU J11/J21 breakout box	1	SU	NA	01	NA
10.	HV load resistor	1	Battel Engr	BE02598169	01	NA
11.	Banana plug patch cables	20	Pasternak	NA	NA	NA
12.						
13.						
14.						
15.						
16.						

11.0 Equipment Pretest Requirements:

	P/F	Notes:
11.1. Verify P0758 has been run on the Spacecraft Emulator GSE within the past 60 days or since the rack has been moved to the current test location.		Date: Revision:

12.0 Test Connection

Note: *All handling of this DUT shall be performed using ESD control methods, as outlined in MIL-STD-1686. Unit shall be inspected at an ESD certified station. Wrist straps and/or heel grounding straps shall be used.*

Important: **Insure that power is removed from cable assemblies before connecting or disconnecting cable connectors.**

		P/F	Notes
12.1.	Verify that LabView is not running on the S/C emulator PC.		
12.2.	Verify that the front panel of the HP power supply indicates 0.0V output.		
12.3.	Configure the system as shown in Figures 1, and 2.		

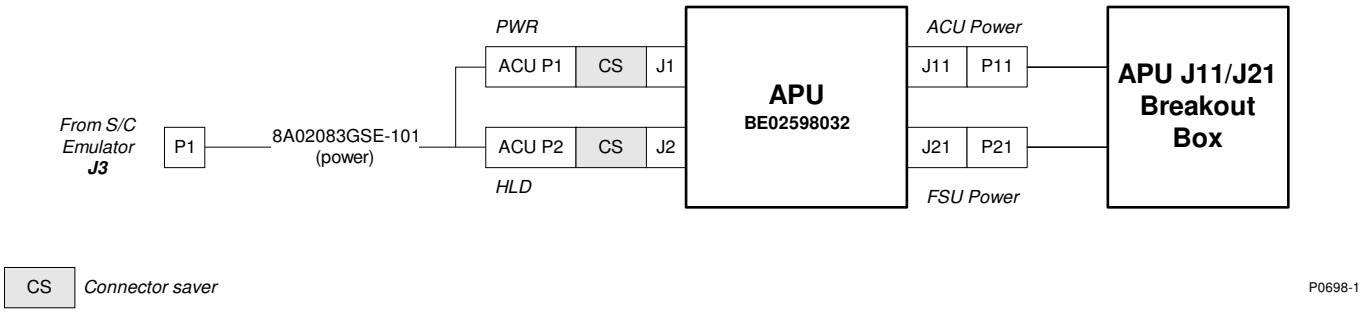

Figure 1: Connection Diagram for ASU tests

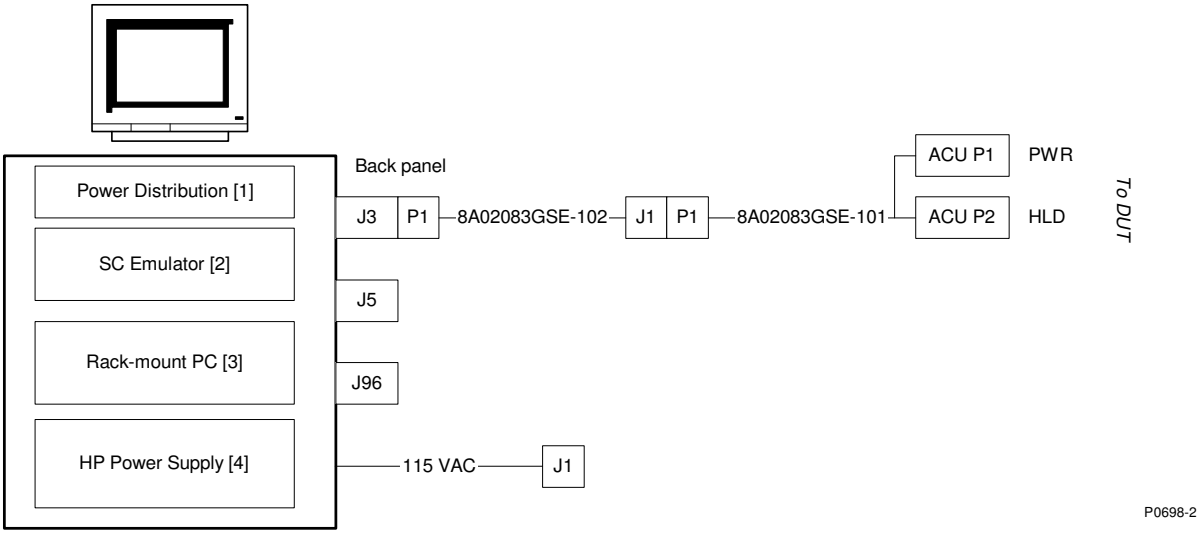

Figure 2: Spacecraft Emulator Wiring Diagram

End of Section

		P/F	Notes
12.4.	Set current limit on HP power supply in S/C emulator rack to 2.0 A A) Close any LabView program that may be running. B) Key in the following sequence on the front panel of the HP supply: "**LOCAL, Function:CURRENT, 2.0, ENTER**"		
12.5.	Restart the LabView *GSE Test* virtual instrument.		
12.6.	Set supply voltage to **28.0 V** on the *GSE test* panel.		

13.0 APU J11 (Aft power) Tests

		P/F	Notes
13.1.	Apply power to the aft supply subsection of the APU by clicking "Aft" on LabView "Power Status" sub panel.		
13.2.	Record indicated main bus current as indicated on HP power supply front panel.		Current:
13.3.	Confirm the following outputs on J11:		

Output Pin	Measured with respect to Pin	Pass Range	Measured Value	P/F
6	4	3.30 ± 0.15 V		
7	4	5.00 ± 0.15 V		
8	4	5.00 ± 0.15 V		
18	4	15.0 ± 0.2		
19	4	-15.0 ± 0.2		
24	25	3.00 ± 0.20		

13.4.	Remove power to the aft supply subsection of the APU by clicking "Aft" on LabView "Power Status" sub panel.	

End of Section

14.0 APU J21 (Fwd power) Tests:

		P/F	Notes
14.1.	In the HLD status sub panel, click “Power Mod 750 A” twice (on then off) and leave it in the off state (this is to synchronize the latching relay in the APU with the LabView system)		
14.2.	In the HLD status sub panel, click “Power Mod 750 B” twice (on then off) and leave it in the off state (this is to synchronize the latching relay in the APU with the LabView system)		
14.3.	Verify the values in the matrix below for the given settings of the “FSU Main” and “FSU Backup” Power Status panel settings.		

LabView Power Status Settings		**Pins on APU J21**					**P/F**
FSU Main	FSU Backup	2	12	11	5	3	
ON	off	+7.1 ± 0.5 V Measured:	+16.2 ± 0.5 V Measured:	-16.2 ± 0.5 V Measured:	+60.5± 1.0 V Measured:	-60.5 ± 1.0 V Measured:	
off	**ON**	+7.1 ± 0.5 V Measured:	+16.2 ± 0.5 V Measured:	-16.2 ± 0.5 V Measured:	+60.5± 1.0 V Measured:	-60.5 ± 1.0 V Measured:	
ON	**ON**	+7.1 ± 0.5 V Measured:	+16.2 ± 0.5 V Measured:	-16.2 ± 0.5 V Measured:	+60.5± 1.0 V Measured:	-60.5 ± 1.0 V Measured:	
Measured w.r.t Pin		1	4	4	4	4	

14.4.	Set “FSU Main” and “FSU backup” to the off position.	
14.5.	Connect the HV resistor load box as indicated in Figure 3	
WARNING: HIGH VOLTAGE ENABLED		
14.6.	With “FSU Main” and “FSU Backup” in the on position, verify t the values in the matrix below for the given settings of the “Power Mod 750A” and “Power Mod 750B” Power Status panel settings.	

LabView HLD Status Settings		**Pins on APU J21**		**P/F**
Power Mod 750A	Power Mod 750B	A1	A2	
ON	off	+750 ± 20 V Measured:	-750 ± 20 V Measured:	
off	**ON**	+750 ± 20 V Measured:	-750 ± 20 V Measured:	
ON	**ON**	+1450 (+40, -30)V Measured:	-1450 (-40, +30)V Measured:	
Measured w.r.t Pin		4	4	

* Measure A1 and A2 using two volt meters in parallel; sum the results.

14.7.	Set “Power Mod 750A” and “Power Mod 750B” to the off position.	
Note: HIGH VOLTAGE IS DISABLED		
14.8.	Set “FSU Main” and “FSU backup” to the off position.	

14.9.	Turn on “Heater” in LabView power status panel.	
14.10.	Verify that the voltage between J21 Pin 6 -> J21 Pin 13 is 12.0 ± 1.0 V	
14.11.	Turn off “Heater” in LabView power status panel.	

End of Section

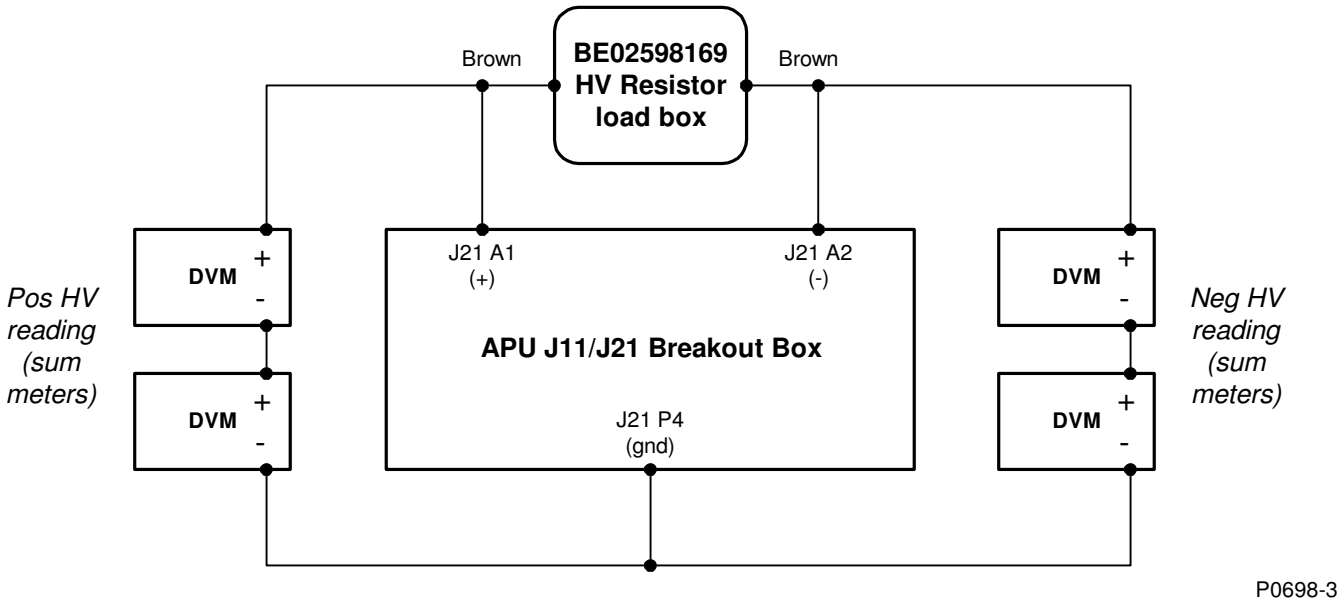

Figure 3: Hookup of meters, load to measure APU HV outputs

15.0 Completion of Procedure:

		P/F	Notes
15.1.	Turn off power via LabView *GSE Test* window; record off time in Power log.		
15.2.	Remove all external cables from DUT		
15.3.	Verify connector mate/demate log entries have been made for DUT for connectors without connector savers installed.		

End of Section

16.0 Certification:

I certify that this procedure was performed in whole and that the data recorded above is complete and accurate.

Test Engineer		Date	

This is to certify that the information obtained under this test procedure is as represented and the documentation is completed and correct.

GSS Representative		Date	
Quality Assurance		Date	