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Gravity Probe B Relativity Mission

BOARD-LEVEL TEST PROCEDURE FOR THE GYROSCOPE SUSPENSION SYSTEM (GSS) MUX/OSCILLATOR/CHARGE CTRL (MUX) BOARD

PWA 8A01883 Rev C S/N: [ ]

GP-B Procedure
P0607 Rev -

Prepared by: William Bencze Date
PWA Responsible Engineer

Approved by: William Bencze Date
RE, Gyroscope Suspension System (GSS) Group

Approved by: Dorrene Ross Date
GP-B Quality Assurance

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1.0 Revision History

Rev Level	Comments/notes	Date	Revised By
-	First release of this test procedure	1-May-00	B. Bencze

2.0 Scope:

This procedure details the board-level electrical functional tests on the GSS MUX/Oscillator/Charge Control (MUX) card. No mechanical or thermal stress testing shall be performed at this time.

This test plan has been written to be run with the GSS "Gold System" test fixture – an electrically and interface equivalent of the GSS flight units. In General, the Device Under Test (DUT) shall be inserted into the Gold System in place of the equivalent Gold System card, any additional electrical connections to the Gold System shall be made, and a set of software-based and possibly manual tests will be run on the board. Upon successful completion of this procedure, this board is considered electrically functional.

All data recorded during this test is recorded in this document; each test of a board will use its own copy of this procedure, and will be identified by serial number on the cover sheet.

3.0 Reference Documents

3.1. GSS Gold System Hardware and Software Configuration Standard, P0663

3.2. PWA Drawing, GSS MUX board, 8A01883

3.3. PWB Drawing, GSS MUX board, 8A01889

3.4. PWA schematic, PC610A gold system test card.

3.5. PWA schematic, PC620A gold system test card.

3.6. Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment, MIL-STD-1686

4.0 Test Facilities

HEPL Room 127, Stanford University

5.0 QA Provisions:

5.1. This procedure shall be conducted on a formal basis to its latest approved and released version. The QA Program Engineer (D. Ross) and the ONR representative (E. Ingraham) shall be notified 24 hours prior to he start of this procedure. QA may monitor the execution of all or part of this procedure should they elect to do so.

Date/time:_____	Date/time:_____
GP-B QA (D. Ross)	ONR (E. Ingraham)

5.2. Upon completion of this procedure, the GSS manager and the GP-B QA manager shall certify her/his concurrence that the procedure was performed and accomplished in accordance with the prescribed instructions by signing and dating his approval at the end of this procedure.

6.0 Test Personnel

This test procedure is to be conducted only by the following personnel:

6.1. William Bencze

6.2. Lo Van Ho

7.0 General Instructions

7.1. Redlines can be initiated by the test personnel listed in Section 6.0 and must be approved by QA.

7.2. Test operators shall read this procedure in its entirety and resolve any apparent ambiguities prior to beginning this test.

7.3. Any nonconformance or test anomaly should be reported by a Discrepancy Report. Refer to the Quality Plan, P0108, for guidance. Do not alter or break test configuration if a test failure occurs; notify quality assurance.

7.4. Only the following persons have the authority to exit/terminate this test or perform a retest: Test operators listed in Section 6.0 and GP-B QA.

7.5. In this document, “Perform Flight S/W system test commands:” means to prepare the test system software as described in P0670 Board-Level Test Software Operational Procedure, and then issue the listed commands according to the procedure described in P0670.

8.0 Hardware Safety Requirements:

8.1. This assembly is ESD sensitive; special care shall be exercised per the “Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment”, MIL-STD-1686

8.2. Ensure that power is removed from cable assemblies before connecting or disconnecting cable connectors.

8.3. Examine all mating connectors before attempting to mate them. Remove any foreign particles. Look for any damaged pins or sockets. Do not force the coupling action if excessive resistance is encountered. Ensure that key-ways are aligned when mating connectors.

9.0 Equipment Pretest Requirements:

9.1. The GSS Gold System in which this board is to be tested must have passed successfully the P0663 – Gold System Certification Procedure prior to the start of this test. Record the Gold System serial number and date of its certification, below

GSS Gold System	SN:	
	Date of Certification	
	Configuration (circle one)	Full Partial

10.0 Additional Test Equipment

The following support hardware, test equipment, or software will be used and the applicable information for the instruments shall be recorded below. Hand-written additions to this list may be made in the space provided.

Equipment Description	Make	Model	SN	Cal Due
1. Multimeter	Fluke			
2. Multimeter	Fluke			
3. Multimeter	Fluke			
4. Gain/Phase meter	HP			
5. Signal Generator	SRS			
6. Oscilloscope	Tek			
7. Triple output power supply	HP			
8. PC620 gold system test card	SU	Rev A		NA
9. PC610 gold system test card	SU	Rev A		NA
10. Gold system Fwd backplane with banana-plug power port	SU PC400	NA	002-GS	NA
11. BNC-to-Pomona mini-clip test cable, 3’	SU fab	NA	NA	NA
12. 5 ea 100 kohm tuning pot.	SU	NA	NA	NA
13. 1 ea 200 kohm tuning pot.	SU	NA	NA	NA
14. Bolt-up FSU enclosure	LMMS	NA	NA	NA
15. BNC patch cables, as required	Various	NA	NA	NA
16. Meter test leads, as required	Various	NA	NA	NA

11.0 Device Under Test (DUT):

Record the serial number of the Device Under Test, or DUT.

PWA 8A01883 GSS MUX Card	SN:	
Test Operator:	Name:	
Start of test:	Date:	

12.0 Pre-test visual inspection.

Note: All handling of this PWA shall be performed using ESD control methods, as outlined in MIL-STD-1686. Unit shall be inspected at an ESD certified station. Wrist straps and/or heel grounding straps shall be used.

P/F	Test/Activity	Notes
	12.1. Remove PWA from storage container.	
	12.2. Verify that the PWA has been tuned per procedure P0711.	
	12.3. Verify proper value of R2 installed per traveller.	
	12.4. Verify proper value of R6 installed per traveller.	
	12.5. Verify proper value of R26 installed per traveller.	
	12.6. Verify proper value of R30 installed per traveller.	
	12.7. Verify proper value of R20 installed per traveller.	
	12.8. Verify proper value of R24 installed per traveller.	
	12.9. Verify proper value of R36 installed per traveller.	
	12.10. Verify proper value of R42 installed per traveller.	
	12.11. Verify proper value of R28 installed per traveller.	
	12.12. Verify proper value of R74 installed per traveller.	
	12.13. Verify proper value of R46 installed per traveller.	
	12.14. Verify proper value of R47 installed per traveller.	
	12.15. Verify R15 is not installed.	
	12.16. Verify R41 is not installed.	

13.0 Pre-Insertion Static Electrical Tests:

Note: All handling of this PWA shall be performed using ESD control methods, as outlined in MIL-STD-1686. Unit shall be inspected at an ESD certified station. Wrist straps and/or heel grounding straps shall be used.

13.1. Power circuits isolation check

A. Set meter to "ohms", record indicated resistance between the indicated circuit points.
B. Note orientation of (+) and (-) leads on meter.
C. Use gold-tipped Pomona test probes for all measurements.
D. After leads are in contact with the PWA, wait 30 seconds for meter reading to stabilize before recording measurement.

P/F	Test/Activity	Pass Criteria	Measurement
	13.1.1. TP22 (+) to TP25 neg lead (-)	> 100 kohm	Value
	13.1.2. TP23 (+) to TP25 neg lead (-)	> 100 kohm	Value
	13.1.3. TP24 (+) to TP25 neg lead (-)	> 100 kohm	Value

14.0 In-System Testing – Flight Configuration

Note: Tests run in this section are run with the hardware in "flight" configuration: no external test equipment or cables. The tests here use only the onboard diagnostic facilities of the GSS hardware. These will be the equivalent of the on-orbit tests of this system.

15.0 This section not applicable

15.0 In-System Testing – Ground Test Configuration

Note: Tests run in this section require the addition of test cables and external test hardware. They are used to verify the board functioning of the board in fine detail, and are only used at the time of board-level test and acceptance. These may be considered "Engineering Confidence Tests".

15.1. Gold System Configuration

This board-level test does not require any of the services of the aft GSS unit or many of the services of the forward GSS unit. The gold system will be partially disassembled to facilitate this test.

P/F	Test/Activity	Notes
	15.1.1. Remove all gold system function cards from the forward GSS enclosure; return them to their protective ESD packaging.	
	15.1.2. Install Gold System backplane and PC610/620 test cards into a bolt-up frame GSS forward enclosure. Remove side panel to expose the component side of the DUT when installed.	
	15.1.3. Connect backplane pigtail to power supply.	
	15.1.4. Install DUT into its proper slot in the forward enclosure per P0663. *(note: no FSU covers are needed for this test)*	

15.2. Configure PC620:

P/F	Test/Activity	Notes
	15.2.1. Connect *BNC-to-pomona clip cable* to frequency generator.	
	15.2.2. Connect red (+) clip to PC620 TP84 *(FSU_CK34K1_A)*	
	15.2.3. Connect black (-) clip to PC620 AGND TP	

15.3. Gain/Phase meter setup

P/F	Test/Activity	Notes
	15.3.1. CH A: 2mV-20V setting	
	15.3.2. FREQ RANGE: 10 – 10 kHz	
	15.3.3. AMPLITUDE FNC: A	
	15.3.4. PHASE REF: A	
	15.3.5. CH B: 2mV-20V setting	

15.4. Function generator setup

P/F	Test/Activity	Notes
	15.4.1. Freq: 34.100 kHz	
	15.4.2. Amplitude: 1.0 Vpp	
	15.4.3. Waveform: SIN	

15.5. Power on:

P/F	Test/Activity	Notes
	15.5.1. Apply power to the FSU enclosure.	

15.6. Oscillator Tests:

P/F	Test/Activity	Notes
	15.6.1. Verify signal at X_OSC (PC620) is phase-locked to the input using the scope.	
	15.6.2. Verify that the signal at X_OSC (PC620) remains locked for frequencies ± 50 Hz from 34,100 Hz.	
	15.6.3. Record the DC value of TP10 with an external sync frequency of 34,050 Hz.	Value:
	15.6.4. Record the DC value of TP10 with an external sync frequency of 34,100 Hz.	Value:
	15.6.5. Record the DC value of TP10 with an external sync frequency of 34,150 Hz.	Value:
	15.6.6. Using a multimeter set to AC volts, verify that the amplitude of X_OSC (PC620) is **354 ± 0.010 mV RMS.** *(1 V p-p)*	Value:
	15.6.7. Using a multimeter set to AC volts, verify that the amplitude of Y_OSC (PC620) is **354 ± 0.010 mV RMS.** *(1 V p-p)*	Value:
	15.6.8. Using a multimeter set to AC volts, verify that the amplitude of Z_OSC (PC620) is **354 ± 0.010 mV RMS.** *(1 V p-p)*	Value:
	15.6.9. Using the gain/phase meter, verify that the phase difference between X_OSC (Ch A) and Y_OSC (Ch B) is **-120.0 ± 1.0 degrees.**	Value:
	15.6.10. Using the gain/phase meter, verify that the phase difference between X_OSC (Ch A) and Z_OSC (Ch B) is **+120.0 ± 1.0 degrees.**	Value:
	15.6.11. Verify that a 34.1 kHz square wave is present on TP58 – 34CK_D (PC620).	

15.7. Charge Control Drive Test:

P/F	Test/Activity	Notes
	15.7.1. Install jumper 2-3 location on JP39 on PC620 *(P3_EN; LED off)*	
	15.7.2. Install jumper 2-3 location on JP36 on PC620 *(M3_EN; LED off)*	
	15.7.3. Measure and record value of PC620 TP80 (C_ETRODE). Verify it is **0.000 ± 0.010 V DC** with respect to TP17 (SIG_AGND)	Value:
	15.7.4. Install jumper 1-2 location on JP39 on PC620 *(P3_EN; LED ON)*	
	15.7.5. Install jumper 2-3 location on JP36 on PC620 *(M3_EN; LED off)*	
	15.7.6. Measure and record value of PC620 TP80 (C_ETRODE). Verify it is **3.0 ± 0.2 V DC** with respect to TP17 (SIG_AGND)	Value:
	15.7.7. Install jumper 2-3 location on JP39 on PC620 *(P3_EN; LED off)*	
	15.7.8. Install jumper 1-2 location on JP36 on PC620 *(M3_EN; LED ON)*	
	15.7.9. Measure and record value of PC620 TP80 (C_ETRODE). Verify it is -**3.0 ± 0.2 V DC V DC** with respect to TP17 (SIG_AGND)	Value:

15.8. Control Signal Multiplexer Test:

Note: Logical values and LED status: On = "1", Off = "0".

P/F	Test/Activity	Notes
	15.8.1. Set JP31 (MODE0) on PC610 to "1"	
	15.8.2. Set JP34 (MODE1) on PC610 to "1"	
	15.8.3. Set JP15 (P_BU_SEL) on PC610 to "0" (Prime)	

	15.8.4. Measure and record resistance between DA_X1 and TP52 (X1_MUX_OUT) on PC 620. **Pass if < 1 ohm.**	Value:
	15.8.5. Measure and record resistance between TP20 (X1_BU) and TP52 (X1_MUX_OUT) on PC620. **Pass if > 1 meg-ohm.**	Value:
	15.8.6. Measure and record resistance between DA_X2 and TP56 (X2_MUX_OUT) on PC 620. **Pass if < 1 ohm.**	Value:
	15.8.7. Measure and record resistance between TP25 (X2_BU) and TP56 (X2_MUX_OUT) on PC620. **Pass if > 1 meg-ohm.**	Value:
	15.8.8. Measure and record resistance between DA_Y1 and TP60 (Y1_MUX_OUT) on PC 620. **Pass if < 1 ohm.**	Value:
	15.8.9. Measure and record resistance between TP30 (Y1_BU) and TP60 (Y1_MUX_OUT) on PC620. **Pass if > 1 meg-ohm.**	Value:
	15.8.10. Measure and record resistance between DA_Y2 and TP64 (Y2_MUX_OUT) on PC 620. **Pass if < 1 ohm.**	Value:
	15.8.11. Measure and record resistance between TP35 (Y2_BU) and TP64 (Y2_MUX_OUT) on PC620. **Pass if > 1 meg-ohm.**	Value:

	15.8.12. Measure and record resistance between DA_Z1 and TP68 (Z1_MUX_OUT) on PC 620. **Pass if < 1 ohm.**	Value:
	15.8.13. Measure and record resistance between TP40 (Z1_BU) and TP68 (Z1_MUX_OUT) on PC620. **Pass if > 1 meg-ohm.**	Value:
	15.8.14. Measure and record resistance between DA_Z2 and TP72 (Z2_MUX_OUT) on PC 620. **Pass if < 1 ohm.**	Value:
	15.8.15. Measure and record resistance between TP45 (Z2_BU) and TP72 (Z2_MUX_OUT) on PC620. **Pass if > 1 meg-ohm.**	Value:

P/F	Test/Activity	Notes
	15.8.16. Set JP15 (P_BU_SEL) on PC610 to “1” (Backup)	

	15.8.17. Measure and record resistance between DA_X1 and TP52 (X1_MUX_OUT) on PC 620. **Pass if > 1 meg-ohm.**	Value:
	15.8.18. Measure and record resistance between TP20 (X1_BU) and TP52 (X1_MUX_OUT) on PC620. **Pass if < 1 ohm.**	Value:
	15.8.19. Measure and record resistance between DA_X2 and TP56 (X2_MUX_OUT) on PC 620. **Pass if > 1 meg-ohm.**	Value:
	15.8.20. Measure and record resistance between TP25 (X2_BU) and TP56 (X2_MUX_OUT) on PC620. **Pass if < 1 ohm.**	Value:
	15.8.21. Measure and record resistance between DA_Y1 and TP60 (Y1_MUX_OUT) on PC 620. **Pass if > 1 meg-ohm.**	Value:
	15.8.22. Measure and record resistance between TP30 (Y1_BU) and TP60 (Y1_MUX_OUT) on PC620. **Pass if < 1 ohm.**	Value:

	15.8.23. Measure and record resistance between DA_Y2 and TP64 (Y2_MUX_OUT) on PC 620. **Pass if > 1 meg-ohm.**	Value:
	15.8.24. Measure and record resistance between TP35 (Y2_BU) and TP64 (Y2_MUX_OUT) on PC620. **Pass if < 1 ohm.**	Value:
	15.8.25. Measure and record resistance between DA_Z1 and TP68 (Z1_MUX_OUT) on PC 620. **Pass if > 1 meg-ohm.**	Value:
	15.8.26. Measure and record resistance between TP40 (Z1_BU) and TP68 (Z1_MUX_OUT) on PC620. **Pass if < 1 ohm.**	Value:
	15.8.27. Measure and record resistance between DA_Z2 and TP72 (Z2_MUX_OUT) on PC 620. **Pass if > 1 meg-ohm.**	Value:
	15.8.28. Measure and record resistance between TP45 (Z2_BU) and TP72 (Z2_MUX_OUT) on PC620. **Pass if < 1 ohm.**	Value:

P/F	Test/Activity	Notes
	15.8.29. Set JP31 (MODE0) on PC610 to “0”	
	15.8.30. Set JP34 (MODE1) on PC610 to “0”	

	15.8.31. Measure and record resistance between AGND and TP52 (X1_MUX_OUT) on PC 620. **Pass if < 1 ohm.**	Value:
	15.8.32. Measure and record resistance between AGND and TP56 (X2_MUX_OUT) on PC 620. **Pass if < 1 ohm.**	Value:
	15.8.33. Measure and record resistance between AGND and TP60 (Y1_MUX_OUT) on PC 620. **Pass if < 1 ohm.**	Value:
	15.8.34. Measure and record resistance between AGND and TP64 (Y2_MUX_OUT) on PC 620. **Pass if < 1 ohm.**	Value:
	15.8.35. Measure and record resistance between AGND and TP68 (Z1_MUX_OUT) on PC 620. **Pass if < 1 ohm.**	Value:
	15.8.36. Measure and record resistance between AGND and TP72 (Z2_MUX_OUT) on PC 620. **Pass if < 1 ohm.**	Value:

15.9. Monitor Signal Multiplexer Test:

Note: Logical values and LED status: On = "1", Off = "0".

	Test/Activity	Notes
	15.9.1. For each of the MUX setting below on PC610, check the indicated input/output relation:	
	15.9.2. Inject sinusoidal input where required into each of the test points noted below. 20 Vpp, 100 Hz.	
	15.9.3. Monitor input and output at the MUX_MON SMA connector on PC610.	

	MM[5..0] (address)	**Signal Name**	**Input (PC620 test points)**	**Pass condition**
	00 0000 (0x00)	Y2_BU	25	Match input
	00 0001 (0x01)	X1_BU	30	Match input
	00 0010 (0x02)	DA_Y2	37	Match input
	00 0011 (0x03)	DA_X1	22	Match input
	00 0100 (0x04)	P14A_VMON	43	Match input
	00 0101 (0x05)	P12A_VMON	28	Match input
	00 0110 (0x06)	PHV_VMON	70	Match input
	00 0111 (0x07)	P13V8_VMON	58	Match input
	00 1000 (0x08)	SIGNAL_AGND	-	equals 0.00 V ± 0.01 V
	00 1001 (0x09)	P5A_REF	-	equals 5.00 V ± 0.05 V
	00 1010 (0x0A)	X1_LV_VMON	51	Match input
	00 1011 (0x0B)	Y2_LV_VMON	63	Match input
	00 1100 (0x0C)	X1_HV_VMON	19	Match input
	00 1101 (0x0D)	Y2_HV_VMON	34	Match input
	00 1110 (0x0E)	X_TEMP_MON	74	Match input
	00 1111 (0x0F)	Z_TEMP_MON	78	Match input

	01 0000 (0x10)	Z2_BU	45	Match input
	01 0001 (0x11)	Y1_BU	30	Match input
	01 0010 (0x12)	DA_Z2	47	Match input
	01 0011 (0x13)	DA_Y1	32	Match input
	01 0100 (0x14)	P5D_VMON	38	Match input
	01 0101 (0x15)	M12A_VMON	23	Match input
	01 0110 (0x16)	FRM_TEMP_MON	66	Match input
	01 0111 (0x17)	M50_VMON	54	Match input
	01 1000 (0x18)	MUX_TEMP_MON	-	equals 3.0 V ± 0.2
	01 1001 (0x19)	OSC_VCO_MON	-	equals DUT TP10
	01 1010 (0x1A)	*MUXAD_TBD_09*	-	*NA*
	01 1011 (0x1B)	*MUXAD_TBD_12*	-	*NA*
	01 1100 (0x1C)	Y1_LV_VMON	59	Match input
	01 1101 (0x1D)	Z2_LV_VMON	71	Match input
	01 1110 (0x1E)	Y1_HV_VMON	29	Match input
	01 1111 (0x1F)	Z2_HV_VMON	44	Match input
	10 0000 (0x20)	X2_BU	25	Match input
	10 0001 (0x21)	DA_Z1	42	Match input
	10 0010 (0x22)	DA_X2	27	Match input
	10 0011 (0x23)	M14A_VMON	48	Match input
	10 0100 (0x24)	P5A_VMON	33	Match input
	10 0101 (0x25)	NHV_VMON	18	Match input
	10 0110 (0x26)	M13V8_VMON	62	Match input
	10 0111 (0x27)	P50_VMON	50	Match input
	10 1000 (0x28)	Z1_BU	40	Match input
	10 1001 (0x29)	CHARGE_ELX_MON	-	equals DUT TP12
	10 1010 (0x2A)	*MUXAD_TBD_11*	-	*NA*
	10 1011 (0x2B)	X2_LV_VMON	55	Match input
	10 1100 (0x2B)	Z1_LV_VMON	67	Match input
	10 1101 (0x2D)	X2_HV_VMON	24	Match input
	10 1110 (0x2E)	Z1_HV_VMON	39	Match input
	10 1111 (0x2F)	Y_TEMP_MON	76	Match input

16.0 Completion of Procedure:

		P/F	Notes
16.1.	Remove power from the FSU enclosure.		
16.2.	Remove PWA from enclosure per P0663 and return to storage container.		

The results obtained in the performance of this test procedure are acceptable.

Test Engineer		Date	

This is to certify that the information obtained under this test procedure is as represented and the documentation is completed and correct.

GSS Representative		Date	
Quality Assurance		Date	