FURTHER EVALUATION of GaAs FETs for CRYOGENIC READOUT

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Abstract

Low-frequency, low-noise, low-power cryogenic electronics to read out photodetectors is being investigated for the star-tracking telescope of the Gravity Probe B spacecraft. We report additional results in evaluating low-frequency "1/f" noise of commercial and non-commercial GaAs field-effect transistors (FETs) at room and liquid-helium temperatures. No correlation was found between noise at these two temperatures. For our dc biasing conditions, the lowest-noise non-commercial GaAs FETs give a typical value of K_f ($\equiv A_f$ x gate area) $\approx 2 \times 10^{-22}$ $V^2 \cdot m^2$; this corresponds to a noise voltage of $\approx$80 nV/$Hz^{1/2}$ at 1 Hz for a gate area of 3×10^4 μm^2, only a factor of $\approx$3 higher than the best Si JFETs of comparable gate area operated at their optimum temperature. RTSs (random telegraph signals) were observed for many GaAs MESFETs at 4 K, for gate areas up to $\approx$5000 μm^2. We also examined low-frequency "1/f" noise in relation to FET materials, processing, and pinch-off voltage but the results were inconclusive.

1. INTRODUCTION & BACKGROUND

We are continuing to develop cryogenic readout electronics for the Gravity Probe B (GPB) experiment, which will test relativity theory by measuring minute precessions of gyroscopes in a spacecraft orbiting the Earth.[1-3] The heart of this spacecraft is an assembly comprising the precision superconducting gyroscopes and a star-tracking telescope, all cooled by liquid helium to $\approx$2 K. The telescope will provide an extremely precise reference direction for determining the gyroscope precessions.[4]

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 0-8194-1182-5/93/$6.00

We have been evaluating a cryogenic photodetector system for the GPB telescope, based on semiconductor photodiodes in combination with low-noise, low-power buffer/readout preamplifiers also operating in the cryogenic environment. The proposed readout circuit (Figure 1) is a standard charge integrator with reset, using field-effect transistors (FETs); eight separate readout circuits would be used on the telescope.

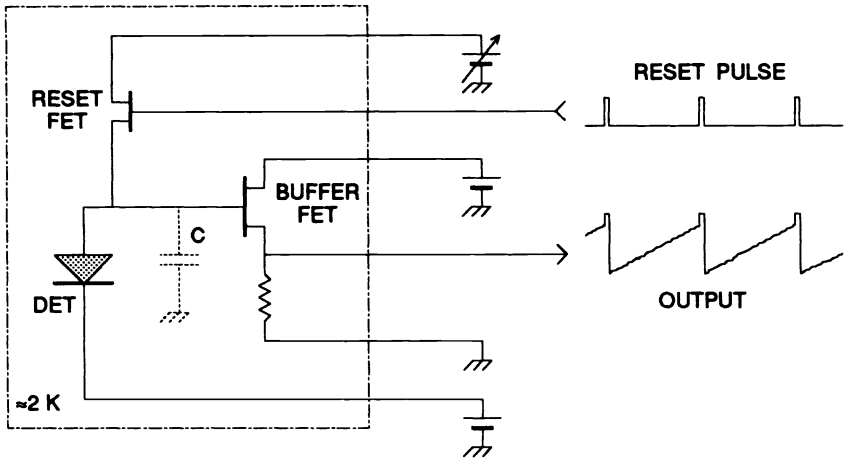


Figure 1 - Proposed charge-integration circuit, with buffer transistor and reset transistor, to operate in a liquid-helium temperature environment at ≈2 K. Photodiode (DET) current accumulates on circuit capacitance represented by C, and is periodically reset.

Finding transistors with a suitable combination of characteristics for applications of this type, particularly for temperatures below ≈40 K, has been an ongoing problem in cryogenic instrumentation; typically Si JFETs or MOSFETs are used. The required characteristics and alternatives were presented previously.[5] The key requirements specific to our application are

1) low input (gate-leakage) current, imposed by the expected photocurrent and photodiode impedance, which is effectively purely capacitive and of small value (a few pF) for our operating conditions,

2) sufficiently low noise at low frequency (<~10 kHz) to meet our goal of readout system noise being dominated by photon noise,

3) low power dissipation (~10 – 100 μW per readout circuit), for acceptable heat load and mechanical distortion of the telescope from temperature differences.

As described previously, one class of semiconductor devices we have chosen to evaluate is the GaAs FET, which has seen considerable investigation and application at cryogenic temperatures for the UHF & microwave frequency ranges, and also appears promising for low-frequency cryogenic operation.

Our initial survey of GaAs FETs, summarized in Reference 5, demonstrated their basic functionality at cryogenic temperatures, as had been reported previously by others, and provided a general idea of low-frequency noise characteristics, both for commercially available GaAs FETs and for test and custom GaAs FETs from several sources. This paper reports additional investigations during the past year, intended to extend and more systematically examine the characteristics of GaAs FETs at liquid-helium temperatures.

2. DESCRIPTION of GaAs FETs

As before, all GaAs FETs considered in this paper are n-channel, depletion-mode; all are MESFETs except for two JFETs from Aerojet. For reasons explained previously,[5] we concentrated on relatively long gate GaAs FETs ($\geq\approx 1$ μm) rather than those designed for microwave frequencies. Gate sizes are always given as length x width (L_g x W_g).

Our recent investigations emphasized non-commercial GaAs FETs, obtained as test chips (used for process control) and as custom FETs, from the sources listed in Table I. These non-commercial GaAs FETs are referred to as "foundry" FETs in this paper. A basic description of the materials and fabrication is also indicated in Table I and discussed later.

A limited number of additional noise measurements were made on commercial GaAs MESFETs from NEC. These are dual gate; for all measurements reported here the two gates were connected together to simulate a longer gate as suggested by previous investigators,[6-8] and the devices were then measured as if they were single-gate FETs.

Table I - "Foundry" GaAs JFETs and MESFETs Evaluated

Manufacturer[a]	Abbrev-iation[b]	Description	Fabrication[c]	Gate dimensions L_g x W_g (μm)
Aerojet	AE	Custom JFETs	Epitaxial junction, MBE on LEC substrates[9]	48, 88 x 200
ITT-GTC	IT	Process Control Monitor MESFETs	MSAG process[10,11]	20 x 1712
Microwave Technology	MT	"Fat" MESFETs (6 lots)	Epitaxial, Arsine VPE on HB or LEC substrates[d]	60 x 90
TriQuint	TQ	Custom MESFETs	D-FETs from QED/A process	2, 25 x 5
TriQuint	TG	Custom cryogenic MESFETs for INFN[12]	D-FETs from QED/A process	1, 2, 5, 10 x 50
TriQuint	TV	Custom cryogenic MESFETs for Top-Vu[13]	D-FETs from QED/A process	5, 10, 15, 20, 100 x 3
Vitesse	VI	Process control monitor and "fat" MESFETs	H-GaAs-II	1.2, 3 x 10; 100 x 160
Vitesse/MOSIS	VM	Custom MESFETs[14]	H-GaAs-II	2, 4, 8, 16 x 50

[a]Those added in this paper are in *italics*.

[b]For Figure 5

[c]Except for Aerojet and Microwave Technology, all FETs are made by ion implant of Si into LEC GaAs wafers.

[d]These GaAs substrates are described later in Section 5.

3. MEASUREMENT PROCEDURE

Noise measurements were made at 300 K and 4 K; we assume that the FET characteristics for ≈2 K operation will be essentially the same as those we measure at 4 K because the effective temperature of the FET's active region will be significantly higher in either environment. Measurements at 4 K were made by direct immersion of the FETs into liquid helium. The foundry FETs were mounted in open packages, thus the die were directly exposed to the liquid helium. In several experiments the FET was also measured just above the liquid helium, and no difference in noise was observed. When measuring exposed die, at 300 K or 4 K, light was excluded. Except where noted, the noise measurements were made in the same manner as described in Reference 5; however, for recent measurements, an Analog Devices AD745AN JFET/bipolar operational amplifier was used rather than the Texas Instruments TLC2201 CMOS opamp, and several other minor alterations were made in the apparatus and procedure. As before, the output of the noise measurement circuit was fed to a Hewlett Packard 35660A signal analyzer, and also observed on an oscilloscope.

All noise spectra and derived factors presented in this paper are gate (input) referred. For all measurements the gate was grounded for ac over the measured frequency range, thus the measurements are of noise voltage and do not include any contribution from input-referred noise current. System "baseline" noise has not been subtracted from any of the noise spectra. Measured frequency range was 1 Hz to 12.9 kHz, measured in two frequency spans: 1 Hz – 101 Hz and 100 Hz – 12.9 kHz. The A_f values in this paper are averages, obtained from averaging by eye on a plot of $A_f(f) \equiv e_n(f)^2 \times f$, over ≈1 Hz to ≈3 kHz.[15] Since noise spectra frequently deviate from a strict 1/f dependence, these average A_f values should be regarded with caution.

As before, during all our measurements we found no device failures that could be clearly attributed to temperature cycling. However, two of the exposed foundry FETs exhibited a factor ≈2 – 3 increase in noise over the course of a year.

4. FET BIASING & TRANSCONDUCTANCE

For all measurements V_{ds} = 0.6 V. To normalize comparisons among FETs of different gate widths, recent noise measurements were made with standard drain current *densities* (drain current/gate width), of $I_d/W_g \approx 20$ μA/μm, 2 μA/μm and 0.2 μA/μm, by choosing an appropriate R_F and adjusting the gate bias, V_{gs}.[5] R_F values between 20 kΩ and 18 MΩ were used to obtain I_d from ≈600 μA down to ≈0.6 μA.

Our standard procedure for noise measurements is to cool the FETs with bias applied, adjusting V_{gs} during cooling to maintain V_{ds} at its set point (0.6 V) and I_d near its nominal value. As expected, cooling from 300 K to 4 K results in a positive shift of V_{gs} towards 0 of ≈0.2 – 0.4 V. If a particular FET is measured for different values of I_d, each measurement is made with a separate cool-down, rather than all during one cool-down.

We find that the biasing conditions during cooling can have a significant effect on the level and spectrum of the low-frequency noise at 4 K, presumably a result of the particular charge distribution "frozen-in" as the FET cools. This makes interpretation of noise results difficult, and indicates the importance of knowing and controlling the bias during cooling. The noise spectrum can also be altered while the FET is cold by applying an electrical stress, presumably a result of redistributing the trapped charge, and a counterpart to *collapse* of the dc characteristics.[16]

Overall gain for the measurement circuit (Figure 6 of Reference 5) ranged between ≈10 and ≈400, depending on the particular FET and biasing, from which is calculated the FET's transconductance, g_m (Figure 2). From the Shockley

model,[17] $g_m/W_g = 2\beta_o^{1/2}(I_d/W_g L_g)^{1/2}$, where $\beta_o = 2\varepsilon_s \mu/3d$, ε_s is the permittivity of GaAs (1.16×10^{-12} F/cm at 300 K), μ the carrier mobility, and d the channel thickness. Typical values for μ and d of 2000 $cm^2/V{\cdot}s$ and 0.1 μm, yield $\beta_o \approx 1.5 \times 10^{-4}$ A/V^2, in reasonable agreement with the data of Figure 2.

Many of the FETs show an increase of transconductance at 4 K compared to 300 K, although this is not universal; the situation is complicated in some FETs by a change in output characteristics with cooling which tends to shift our particular biasing point (I_d,V_{ds}) from the saturation region into the linear region. The output (drain) conductance, g_d, may also increase with cooling, with a decrease of the *intrinsic voltage amplification factor*, g_m/g_d.[5-8]

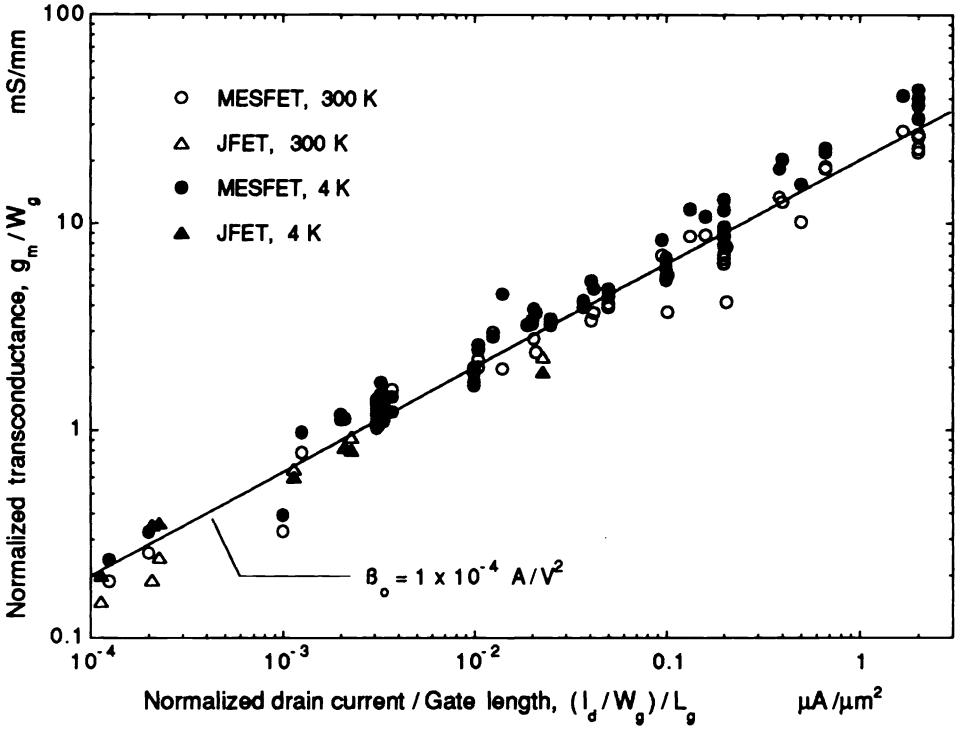


Figure 2 - Normalized transconductance versus normalized drain current divided by gate length. The data fit reasonably well, both at 4 K and 300 K, to a square-root dependence (line), in accord with the Shockley model for long-gate FETs biased in the saturation region.

5. LOW-FREQUENCY NOISE

Source Follower Measurements

Nearly all of our noise measurements have been made in the *grounded-source* configuration referred to above (Figure 6 of Reference 5). To confirm that these measurements are valid for applications using a *source-follower* configuration, such as the proposed Gravity Probe B readout circuit (Figure 1), the noise of several GaAs MESFETs was also measured in a source-follower circuit (Figure 3). As expected, the results from measurements in the source-follower circuit agree well with those measured for the same FETs in the grounded-source circuit (Figure 4), except for the higher noise floor of the source-follower measurement system which is evident above ≈1 kHz for 4 K data.

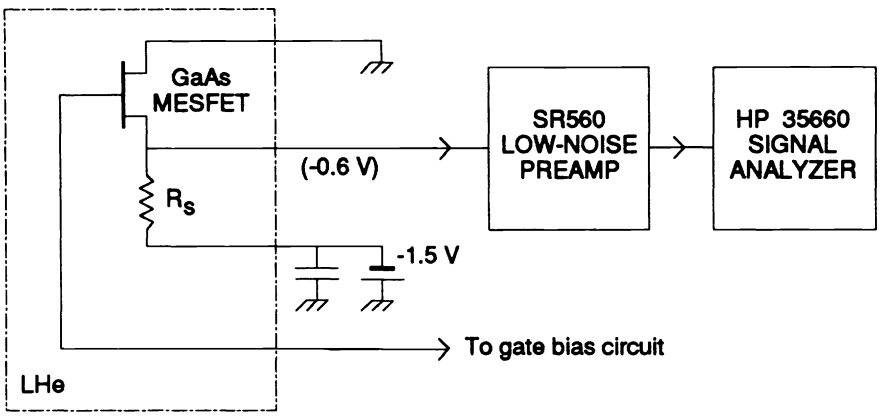


Figure 3 - Source-follower noise measurement circuit. R_S is chosen to give the required I_d. The gate bias circuit is similar to that used for grounded-source measurements (Figure 6 of Reference 5); gate bias is adjusted to give V_{ds} = 0.6 V. For all measurements, the FET substrate is connected to the source. For 4 K measurements, parts within the dashed line are immersed in liquid helium.

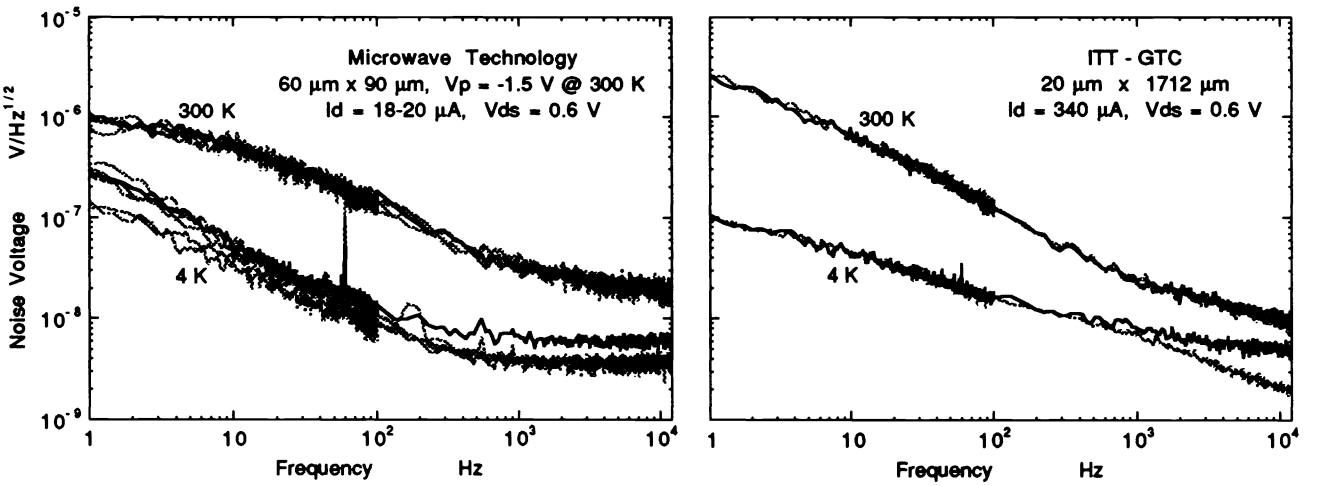


Figure 4 - Comparison between grounded-source and source-follower noise measurements for two GaAs MESFETs. The grounded-source spectra (grey) were measured using the circuit of Reference 5; the source-follower spectra (black) were measured using the circuit of Figure 3 above. The grounded-source spectra in the left graph are from five separate measurements made over six months (five spectra for 4 K, four for 300 K), illustrating the variation in spectra for repeated measurements on the same FET; for 4 K the grounded-source spectra split into two groups at low frequency, probably due to differences in the charge distribution "frozen in" during cooling.

Dependence on Gate Geometry

The 4 K noise-voltage coefficient, A_f, normalized for gate width, W_g, and called $G_f \equiv A_f \times W_g$ is plotted in Figure 5 as a function of gate length, L_g. There was no selection of FETs for this plot: all foundry FETs measured are included, except for a few obviously defective ones. Data for two drain-current density ranges are included, but show no obvious dependence of noise on drain-current density. Although there is considerable scatter in the data, they are consistent with a linear inverse dependence on gate length, and thus a linear inverse dependence of A_f on gate area, as suggested previously,[5,18,19] allowing use of the "figure of merit" $K_f \equiv A_f \times W_g \times L_g$.** The line with slope –1 indicates approximately the lowest noise performance of these GaAs FETs from existing foundry processes that we have measured, with $K_f = 200\ \mu V^2 \cdot \mu m^2$ (this line corresponds to the line in Figure 8 of Reference 5).

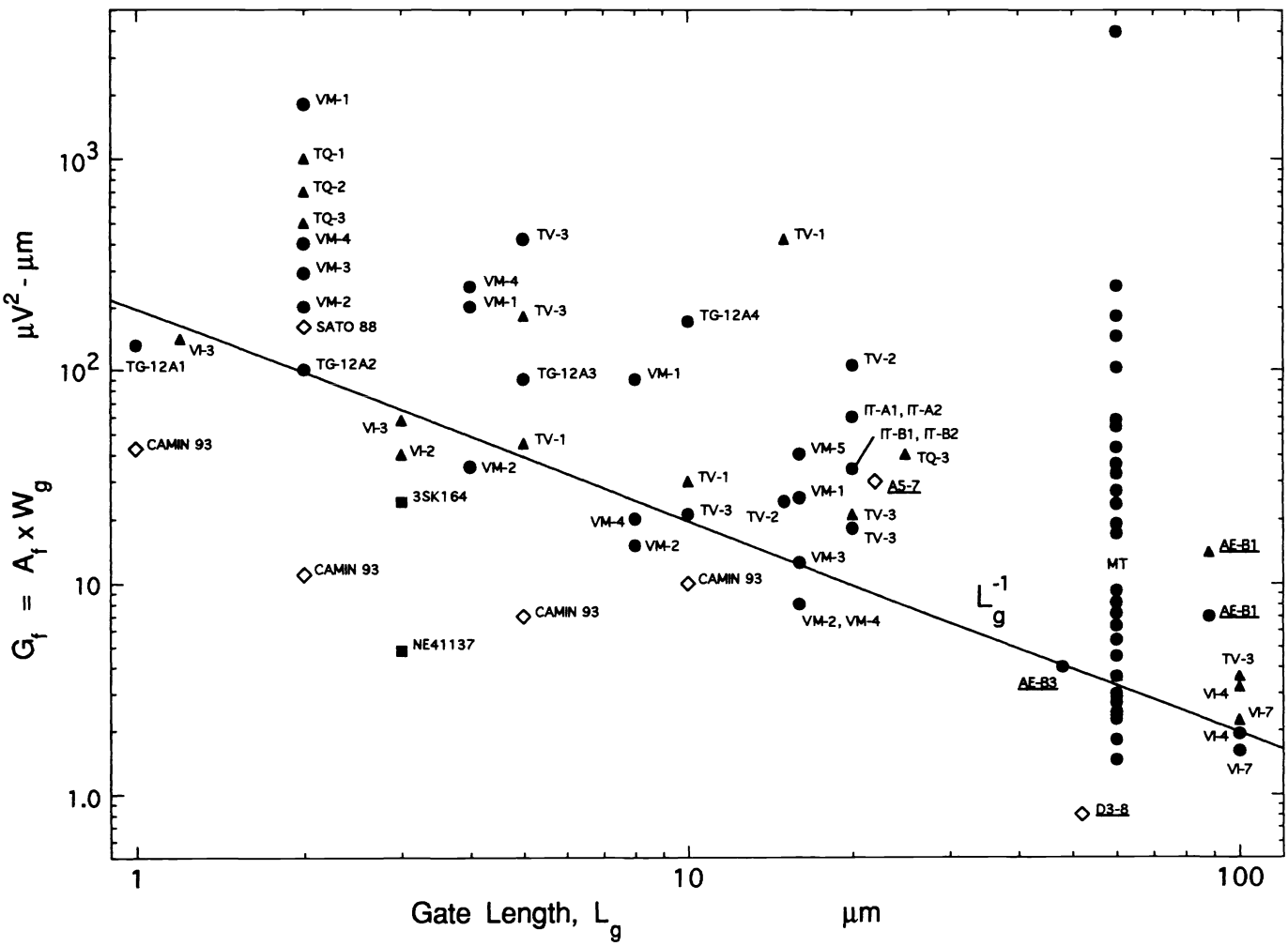


Figure 5 - Normalized 4 K noise coefficient for "foundry" FETs as a function of gate length. Identification of data points consists of a two-letter manufacturer abbreviation (see Table I) followed by a die number (which may include several FETs of different sizes); underlining indicates JFETs (Aerojet), all other points are for MESFETs. The set of points labelled MT at L_g = 60 μm are for Microwave Technology FETs, for which details are presented later. ● $I_d/W_g \approx 0.1 - 0.4$ μA/μm, ▲ $I_d/W_g \approx 1 - 4$ μA/μm, ■ "vintage" commercial GaAs MESFETs, ◇ other published data.

**Also called J_f.[12]

Data reported by others for measurements on GaAs FETs at or near liquid-helium temperatures are also included (◇) for two GaAs JFETs made at Aerojet (A5-7, D3-8),[9] a custom GaAs MESFET made at Hughes (SATO 88),[20] and four custom GaAs MESFETs made by TriQuint for the Istituto Nazionale di Fisica Nucleare (INFN) at the University of Milano (CAMIN 93).[12] For these data I_d and V_{ds} differ from our "standard" values. The INFN data points and the TG- data points are for the same four FETs; however, for the INFN data the biasing was partly optimized for lowest noise, showing that a significant reduction can be obtained; these points also show a minimum in G_f for $L_g \approx 3$ μm.[12]

Early Commercial GaAs MESFETs

Included in Figure 5 are data points (■) for two commercial UHF GaAs MESFETs belonging to INFN: a Sony 3SK164,[6,7] probably made about ten years ago, and an NEC NE41137 (coded M41 = January 1984). In collaboration with INFN, we have measured these same two FETs, and find good agreement between GPB and INFN data (Figure 6). These "vintage" MESFETs have remarkably low noise; in fact, the NE41137 has the lowest noise (normalized for gate area) at 4 K of any GaAs FET we are aware of. Considerably higher noise is reported for later commercial FETs said to be equivalent to these,[22] and for other contemporary commercial GaAs FETs.[5,23]

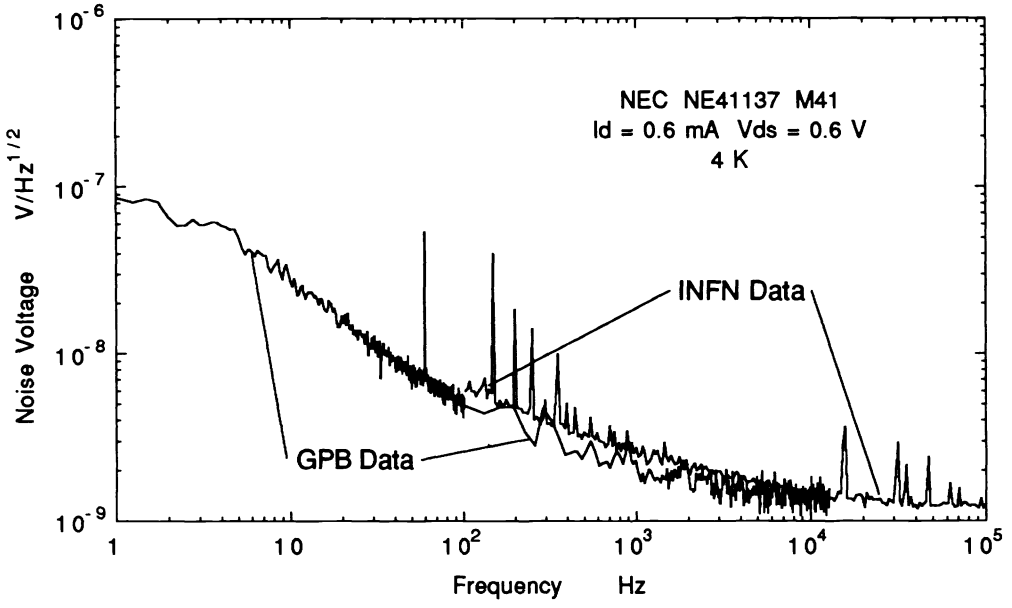


Figure 6 - Input-referred noise spectrum of a commercial GaAs MESFET, NEC type NE41137 (package code M41), which exhibits extremely low noise for a GaAs MESFET. There are two separate overlapping spectra: one measured at the University of Milano (INFN) covering 100 Hz to 100 kHz,[24] using the techniques described in Reference 21, and one measured independently on the same FET at Stanford (GPB) covering 1 Hz to 12.9 kHz, using the techniques described in Reference 5.

This demonstrates the low-noise capability of GaAs FETs at liquid-helium temperature, as low as Si JFETs at their optimum temperature. Unfortunately, we have been unable to find out what accounts for the much lower noise of this particular transistor. Expert opinions are that early FETs were fabricated in GaAs produced by vapor-phase epitaxy (VPE), which is considered to produce high-quality material. However, contemporary "foundry" GaAs MESFETs made using VPE that we have measured do not exhibit noise as low as this "vintage" FET, and we have yet to observe or reproduce this low noise in any other GaAs MESFET, from NEC or elsewhere.

Random Telegraph Signals

For a number of FETs, we have observed a pulse-like signal at the output of the noise measurement circuit, which switches randomly between two or more discrete drain current levels (Figure 7, upper left). Such signals were observed on rare occasions at 300 K, but primarily at 4 K, or at intermediate temperatures—they appear and disappear and change character as the FET is cooled. Also, if present at 4 K they can be altered by changing I_d or V_{ds} or by applying electrical stress.

Although our observations of these signals have been limited and qualitative, their behavior is consistent with random telegraph signals (RTSs),[25] also called *burst* or *popcorn* noise. RTSs are observed in many types of electronic devices, although we are not aware of any reports for GaAs FETs. An RTS originates from the trapping and detrapping of electrons by a single site or small number of sites in or near the channel region of the FET. This causes discrete switching in the channel resistance (and thus in the I_d in our measurement circuit). A common behavior is that at liquid-helium temperature many traps "freeze out" in a typical frequency range, reducing observed "1/f" noise. RTSs are more likely to be observed in transistors with small gate areas; indeed, we observed RTSs often in small FETs; however, we have also observed RTSs in GaAs FETs of relatively large gate area, up to ≈5000 μm^2. Many of the high A_f data points in Figure 5 are from measurements exhibiting an RTS.

An RTS corresponds to a Lorentzian spectrum—flat up to a corner frequency, then falling off as $1/f^2$ (in noise power). We sometimes observed a Lorentzian (Figure 7, upper right and lower right) for devices exhibiting an RTS in the time domain, but in general there was no association between an RTS in the time-domain and a Lorentzian "bulge".

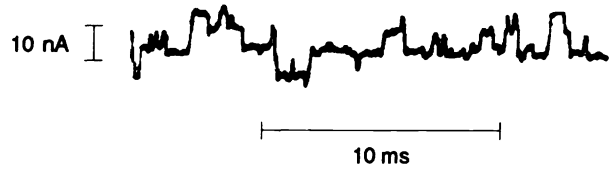
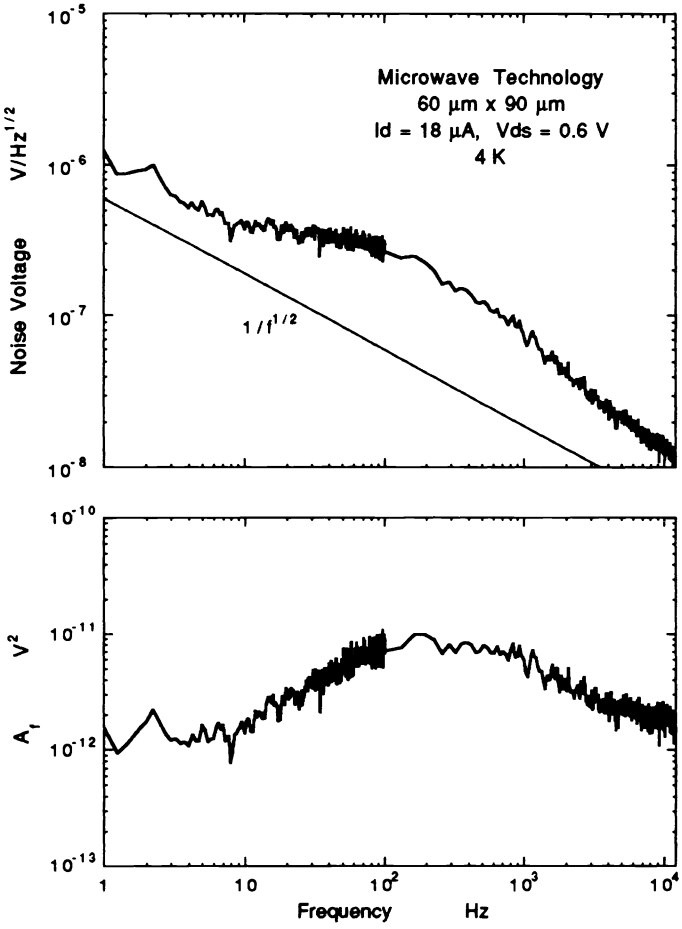


Figure 7 - *Upper left:* Example of oscilloscope trace of the output signal from the noise measurement circuit (Figure 6 of Reference 5). This particular signal shows several drain current levels, differing by ≈5 nA; since $I_d \approx 18$ μA, $\Delta I_d/I_d \approx 0.03\%$, consistent with RTS.[25] *Upper right and lower right:* A noise spectrum from another FET exhibits a Lorentzian component, a "bulge", characteristic of RTS, which is particularly evident in the $A_f(f)$ plot below (a 1/f spectrum would be a straight horizontal line).[15]



Relating Noise at 4 K to Noise at 300 K

Over the frequency range measured here, the noise voltage for GaAs FETs at 4 K is nearly always lower than at room temperature, in accord with previous reports.[5-9,20,21,26] A plot for Microwave Technology FETs (Figure 8, left) shows that the noise power at 4 K can be as high as that at 300 K or less than 1/1000 that at 300 K. As can be seen, 4 K and 300 K noise levels may be weakly correlated for FETs from some wafers; however, overall, there is effectively no correlation. A similar plot for a group of commercial FETs from NEC (Figure 8, right) likewise exhibits no correlation; A_f at 300 K lies between ≈10 and ≈100 μV^2, whereas at 4 K, A_f extends over nearly four orders of magnitude from ≈0.006 to ≈30 μV^2.

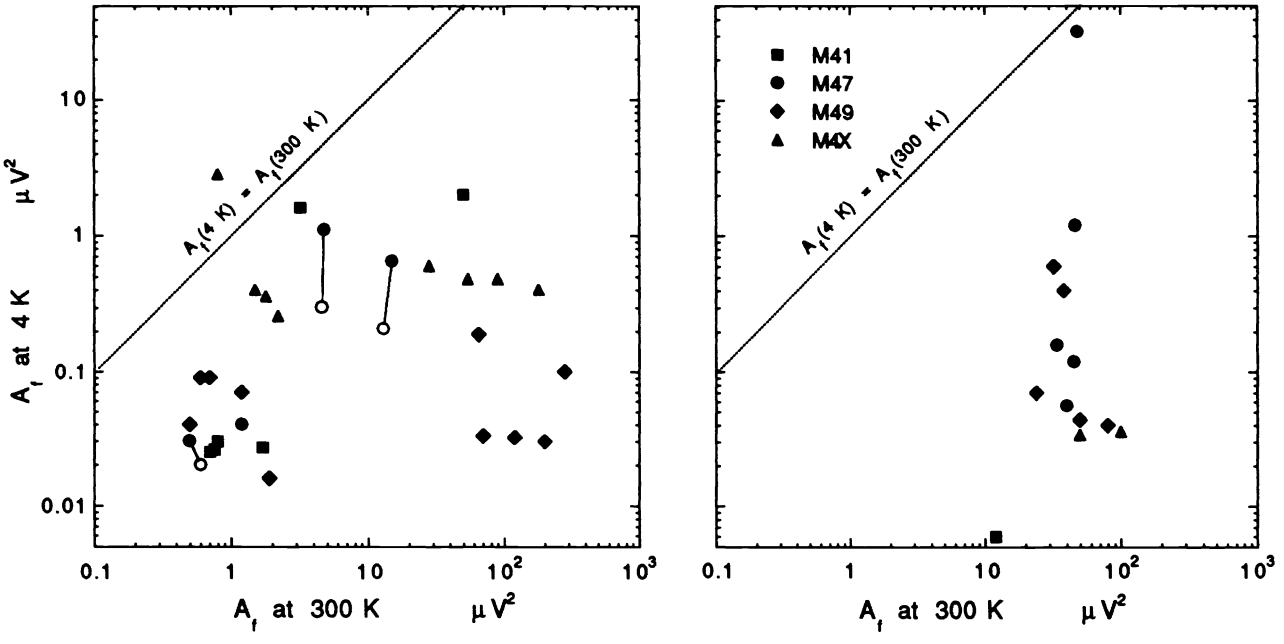


Figure 8 - A_f at 4 K versus A_f at 300 K, showing lack of overall correlation. *Left:* data for 28 Microwave Technology "fat" FETs from different wafers, indicated by different symbols (described later); hollow symbols indicate measurements for a reverse connection (S and D interchanged). $I_d \approx 18$ μA, $V_{ds} = 0.6$ V. *Right:* a similar plot (same scale) for 13 NEC NE41137 GaAs MESFETs with package codes as shown. $I_d \approx 550$ μA, $V_{ds} = 0.6$ V.

Based on these results, from a practical standpoint the room-temperature noise level of a GaAs MESFET cannot be used to predict its liquid-helium temperature noise level, so measurements at liquid-helium temperature are necessary for low-noise selection. Moreover, these data points are for a particular combination of I_d, V_{ds}, and temperature—it is possible that the data points could rearrange completely for other values of these parameters.

As mentioned earlier, the typical decrease in "1/f" noise with cooling is presumed due to a "freezing out" of traps (a shift of their noise to frequencies below the observation range); thus as temperature is decreased from 300 K to 4 K, different sets of traps become dominant for a given frequency range, and it is not surprising that noise at 4 K and noise at 300 K show no strong correlation. Moreover, noise at intermediate temperatures may be higher than either, although we have not made quantitative measurements.

Relating Noise to Materials and Processing

It is intriguing that the lower limit of noise (normalized for gate area) is about the same for all the types of foundry FETs which we have measured, in spite of differences in materials and processing. We have attempted to relate noise to pinch-off voltage, V_p, (and thus I_{dss}) and substrate type, by measuring a number of Microwave Technology "fat" FETs all having the same geometry and processing, but fabricated on different wafers, and having a range of V_p. These FETs are fabricated in arsine-grown VPE layers on two types of GaAs substrates: liquid-encapsulated Czochralski (LEC) or Cr-doped horizontal Bridgman (HB).

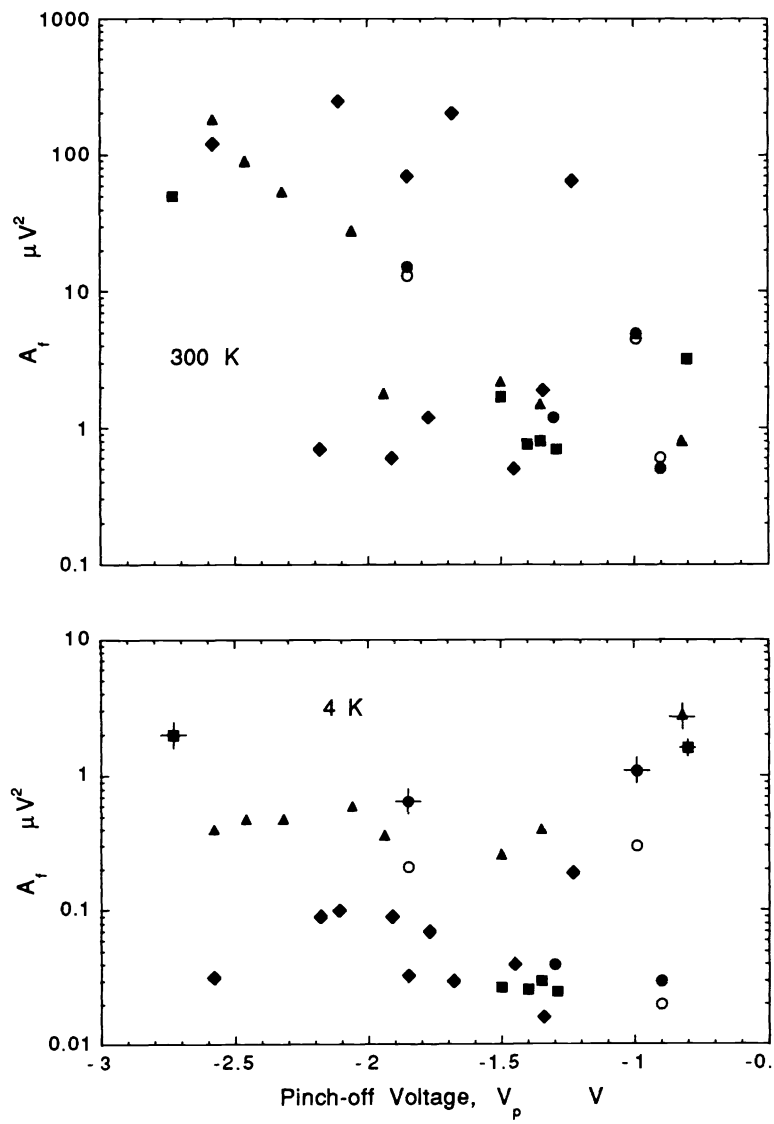


Figure 9 - Noise coefficient, A_f, versus pinch-off voltage, V_p, for 28 "fat" MESFETs from six different wafers (four LEC, two HB). *Top:* 300 K data; *bottom:* 4 K data. For both graphs, V_p is the room-temperature value. For all FETs L_g = 60 µm x W_g = 90 µm, $I_d/W_g \approx 0.2$ µA/µm, V_{ds} = 0.6 V. Hollow symbols indicate measurements for a reverse connection (S and D interchanged). These are the same FETs as in Figure 8 (left) and the symbols have the same meaning. In the bottom graph FETs exhibiting RTS are indicated by a +.

A plot of the A_f values for these FETs (Figure 9) shows no strong correlation with V_p, although there is a tendency toward low noise around $V_p \approx -1.5$ V. FETs from the HB wafers (♦) exhibit lower noise at 4 K ($A_f \approx 0.02$ to $\approx 0.2\ \mu V^2$) more consistently, and we did not observe any RTS in these FETs. FETs from the LEC wafers (■,●) fall into two groups at 4 K: one with low noise ($A_f \approx 0.02$ to $\approx 0.04\ \mu V$), another with high noise associated with observation of RTS. Another lot of FETs is from an LEC wafer with an experimental epitaxial layer (▲) which was found to have an unsatisfactory interface (as determined by room-temperature dc characterization); these FETs show a consistently high $A_f \approx 0.3$ to $\approx 1\ \mu V^2$, although RTS was observed in only one.

Several FETs were measured with source and drain reversed (○), resulting in a slightly different noise spectrum and A_f, particularly at 4 K, implying asymmetry in the distribution of noise generating sites, which is not surprising. The RTS was also altered by the reversed connection.

6. SUMMARY & CONCLUSIONS

We have extended our investigations of commercial and "foundry" GaAs FETs, for application in photodetector readout circuits operating at liquid-helium temperatures. These investigations have yielded no surprising findings, but provide further evidence, alongside the results of other investigators, that GaAs FETs could be useful for low-frequency cryogenic applications, particularly for the temperature range below Si freezout ($<\approx 40$ K), as an alternative to Si JFETs and Si MOSFETs.

Our data for input-referred noise voltage at 4 K are consistent with noise power (A_f) being inversely proportional to gate area, corresponding to a $K_f \equiv A_f \times \text{area} \approx 200\ \mu V^2 \cdot \mu m^2$ for the lowest noise GaAs "foundry" FETs. Table II compares this with typical K_f values for low-noise Si JFETs (commercial) and Si MOSFETs (designed for liquid-helium temperature), although comparing devices of different classes using gate area as the only normalizing factor is of limited validity.

Table II - Comparison of Typical K_f Values

FET Class	GaAs MESFET or JFET	Si JFET	Si MOSFET
Temperature	≈4 K	>≈50 K	≈4 – 10 K
K_f ($\mu V^2 \cdot \mu m^2$)	≈200	≈20[27]	≈200 – 2000[28-30]

We uncovered no clear dependence of "1/f" noise on the type of FET or on materials or processing, nor any correlation between low temperature noise and room-temperature noise.

This evaluation of available GaAs FETs has been useful in surveying their general characteristics at cryogenic temperatures, before embarking on custom development. However, we felt that further work would benefit from better control over materials and designs, and that improvements in low-frequency, cryogenic characteristics might result from using materials and designs other than those currently in use and optimized for high-frequency (microwave) or high-speed digital applications at room temperature.

Therefore, in collaboration with the Istituto Nazionale di Fisica Nucleare at the University of Milano and with Microwave Technology, we have begun design and fabrication of custom GaAs chips. These include a matrix of FETs with geometries systematically varied over a wide range as well as a variety of test structures and integrated readout circuits.

7. ACKNOWLEDGEMENTS

We are greatly indebted to D. Camin, G. Pessina and co-workers at the University of Milano/Istituto Nazionale di Fisica Nucleare for invaluable collaboration on all aspects of this work. We are also indebted to M. Omori of Microwave Technology for valuable discussions and for providing many GaAs MESFETs.

We again thank S. Wong and the Center for Integrated Systems (Stanford Univ.) for continued technical support with device characterization. J. Winston, L. Jostad, J.-Y. Kim, V. Bui and R. Ennulat (GenCorp Aerojet); F. Shoucair (Brown Univ.); J. Naber & D. Miller (ITT-GTC); T. Vu (Top-Vu Technology); R. Savara, A. McCamant and W. Mickanin, (TriQuint Semiconductor); R. Milano, D. Markowski, B.-J. Moon, and K. Rousseau (Vitesse Semiconductor); and R. Mills (NEC/California Eastern Labs) shared their expertise and provided GaAs MESFETs for evaluation.

We also thank M. Shur (Univ. of Virginia); N. Doudoumopoulos (Hughes); P. Solomon (IBM); E. Fossum, T. Cunningham, P. Smith and S. Martin (Jet Propulsion Laboratory); T. Langenstein, J. Turneaure, B. Parkinson, J. Gwo, G. Gutt (Stanford Univ., GPB) for valuable discussions; and P. Prather and the Ginzton Lab. (Stanford Univ.) for technical support. W. Smith, R. Sheasley, A. Jung and J. Hardin (Hewlett Packard), and C. Gonzalez and S. Wang (Stanford Univ., GPB) made vital contributions to data translation and analysis.

This work was supported by NASA under Contract NAS8-36125 out of Marshall Space Flight Center.

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