J. Phys. IV France **8** (1998)

The telescope readout electronics for the Gravity Probe B satellite

H.P. Demroff, S. Babu*, M.R. Bye**, K.L. Coleman, N. Das***, D.B. DeBra****, P.D. Ehrensberger Jr.**, R.P. Farley, D.K. Gill**, J.H. Goebel*****, M. Jhabvala******, A. Kashani*******, E. Romero** and M.T. Sullivan**

Advanced Technology Center, GP-B Lockheed Martin Missiles and Space, Bldg. 251, 3251 Hanover Street, Palo Alto CA 94304, U.S.A.
** Ball Aerospace and Technologies Corp., Boulder, Colorado, U.S.A.*
*** W.W. Hansen Experimental Physics Laboratory, Stanford University, Stanford CA 94305, U.S.A.*
**** Hughes/STX, Lanham, Maryland, U.S.A.*
***** Aeronautics and Astronautics Department, Stanford University, Stanford CA 94305, U.S.A.*
****** Sensors and Instrumentation Branch, NASA Ames Research Center, Moffett Field CA 94305, U.S.A.*
******* NASA Goddard Space Flight Center, Greenbelt, Maryland, U.S.A.*
******* Atlas Scientific, 713 San Conrado Terrace, Sunnyvale CA 94086, U.S.A.*

Abstract. The pointing and stability requirements for the Gravity Probe B (GP-B) Relativity Mission pose a number of challenges for the star-tracking electronics. Because the telescope-gyroscope assembly operates at 2.8 K, the detector circuit's Si JFETs at the telescope focal plane must be thermally isolated and heated to at least 50 K through self-heating or with the aid of heating resistors. We have designed a low noise, thermally stable photodetector circuit that meets the GP-B requirements as well as fabricated an isolator to give the required thermal isolation and mechanical stability. Test results of the detector - isolator assembly are presented.

1. INTRODUCTION

This paper describes the design, fabrication and testing of the telescope readout electronics and thermal isolator for use in the relativity experiment called Gravity Probe B (GP-B). This experiment will measure the geodetic and frame-dragging precessions of four gyroscopes with respect to a guide star. The gyroscopes and star-tracking quartz telescope assembly make up the science instrument of the GP-B satellite payload and will be placed in a 650 km polar orbit. As predicted by Einstein's General Theory of Relativity the calculated precessions are 6.6 arc-seconds/year for the geodetic precession and .042 arc-seconds/year for the frame dragging precession. The goal of this experiment is to measure these precessions to better than .01% and 1% respectively [1].

The candidate guide star, IM Peg, will provide a photocurrent of only 12 fA to each photodiode. The photocurrent is integrated for .1 seconds before being reset. In order to make angle measurements of the required stability, given this expected light intensity, the circuit must be stable to better than 5 photoelectrons / second as the satellite rolls about its axis. The satellite's pitch and yaw are determined by the incident light on two sets of dual photodiodes. A redundant, secondary set provides a backup. The accuracy required for these measurements implies the need for an extremely sensitive and thermally stable set of detector electronics located at the focal plane of the telescope. In addition, a temperature insensitive box of room temperature payload electronics containing additional analog and digital circuitry for the circuit's voltage biases, reset signals and signal amplification is also required.

Figure 1 shows a schematic of the detector circuit. The detector circuit has two stages with a differential current drive as the output. The circuit consists of a dual silicon photodiode, heater, drain and source resistors, a temperature sense diode, feedback capacitors, reset JFETs and low noise silicon n-channel JFETs developed at the Solid State Device Development Branch of NASA Goddard Space Flight Center (GSFC) specifically for GP-B. The components are bonded onto a sapphire substrate.

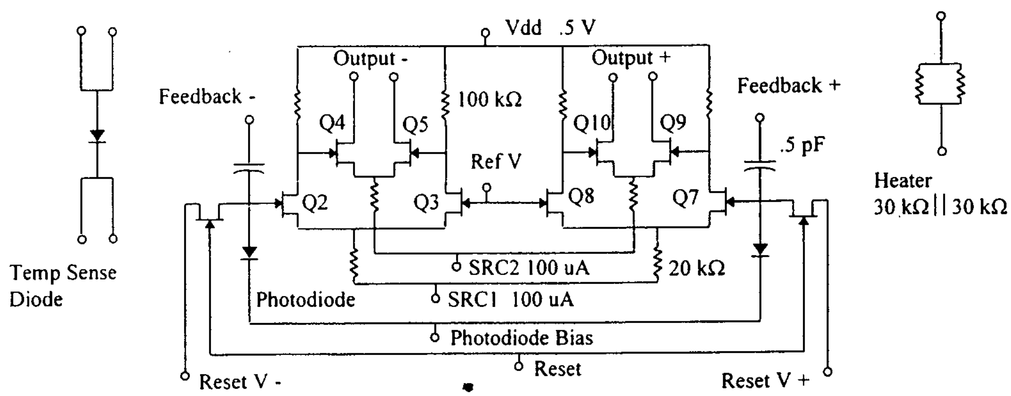


Figure 1: The telescope detector circuit has all 24 components mounted on a sapphire substrate. The circuit has 20 electrical connections and four spares for testing. The temperature sense is a four-point connection. All source resistors are 20 kΩ and all drain resistors 100 kΩ. The two heater resistors are symmetrically located on the sapphire substrate.

With the detector electronics in this 2.8 K environment (in flight) it is necessary to heat the sapphire substrate and JFETs, using 1.5 mW or less, to an operating range between 50 K and 80 K without conducting an excessive amount of heat into the quartz science instrument. In addition, this thermal isolator must also incorporate 24 electrical leads and provide enough mechanical stability to withstand launch loads.

2. DETECTOR CIRCUIT ASSEMBLY AND TESTING

Because it is desirable to have all the components at the same temperature, the circuit is assembled on a sapphire carrier with gold traces. Using standard photolithography, GSFC produces multiple gold patterns of the circuit on a 51 mm diameter, 0.30 mm thick sapphire wafer and the individual circuits are cut out to 9.1 mm diameter with an excimer laser (Resonetics Inc.).

2.1 JFET Measurements and Screening

The requirements for the low noise JFETs call for a Vgs between -1.0 and -1.5 V with 25 uA of drain current and Vds = 1.2 V. The transconductance under these conditions must be greater than .2 mS. The GSFC JFET fabrication process is optimized for low noise performance at cryogenic temperatures. This process minimizes the incorporation of oxygen by growing a low oxygen epi layer and limiting the exposure of the wafer to high temperature processes. The JFETs also have a unique serial number facilitating the screening and tracking process.

After fabrication, the Vgs of nearest neighbor JFETs is measured at room temperature. Refer to Figure 1 for JFET locations. Pairs matching to within 1% are used in the first stage of the circuit (Q2 and Q3, Q8, and Q7). Matching in the second stage is less critical and a match to within 3 % is acceptable. Once the JFETs have been screened for Vgs, an additional selection rule will tend to cancel the effect of the different Vgs values in the circuit. This cancellation is achieved by placing the first stage candidates with the |Vgs| closest to zero in the Q2 position. The JFET with the next lowest Vgs is placed in the Q3 position followed by Q7 and Q8. Similarly the second stage JFETs are ordered with the one with Vgs closest to zero as Q4, then Q5, Q9 and then Q10. The circuit is assembled and wire bonded at GSFC and then shipped to Stanford for electrical testing.

2.2 Detector Circuit Testing

During initial testing it is necessary to adjust the reset voltages (Figure 1, RESV-, RESV+) until the current in the signal and reference drains is equal and the payload electronics output is at zero volts. With the JFETs selected in the manner just described, the required reset voltages change little when cycling between warm and cold operation.

Before the circuit is bonded on top of an isolator assembly the detector is tested at room and liquid nitrogen temperature. One figure of merit is the sense node leakage current at 77 K. Using the payload electronics, we can send the command to open the reset gate and integrate this leakage for long time periods. For 60 second integration times we have measured currents as low as .008 fA.

3. ISOLATOR FABRICATION

The thermal isolator is made from Kapton, utilizing it's mechanical strength and thermal isolation properties. The 24 traces with a 20 nm titanium adhesion layer and 250 nm gold, are patterned on the isolator. For added protection the isolator is then coated with 3 microns of spin-on photodefinable polyimide (DuPont pyralin product PI 2721). Eight traces extend along each of the three legs. Windows in the isolator are etched out to decrease the thermal conductivity. A thorough discussion of the isolator design can be found in a paper by Sullivan, et al. [2]. The isolator is wrapped around a supporting base and glued into place. The three bottom flaps are held in place with press fit pins into the insulating base. See Fig. 2.

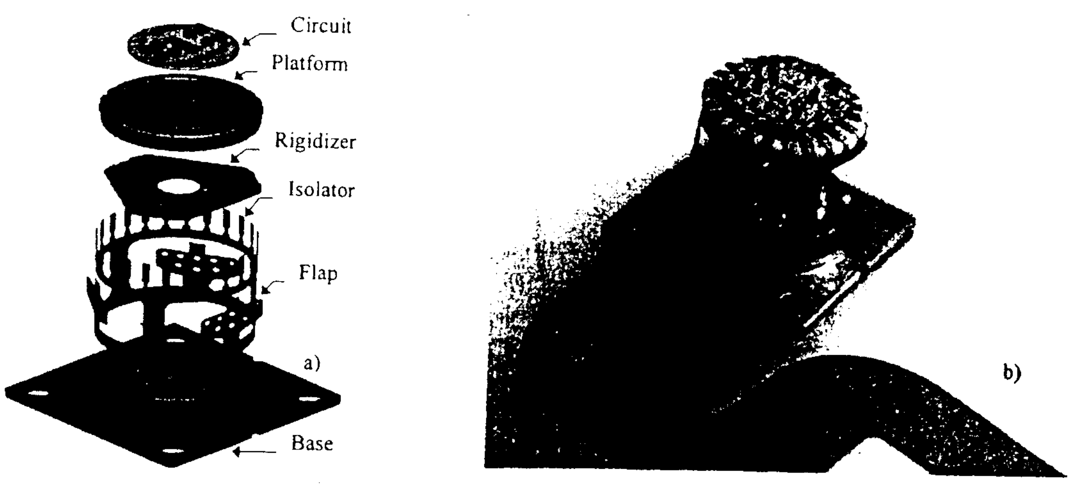
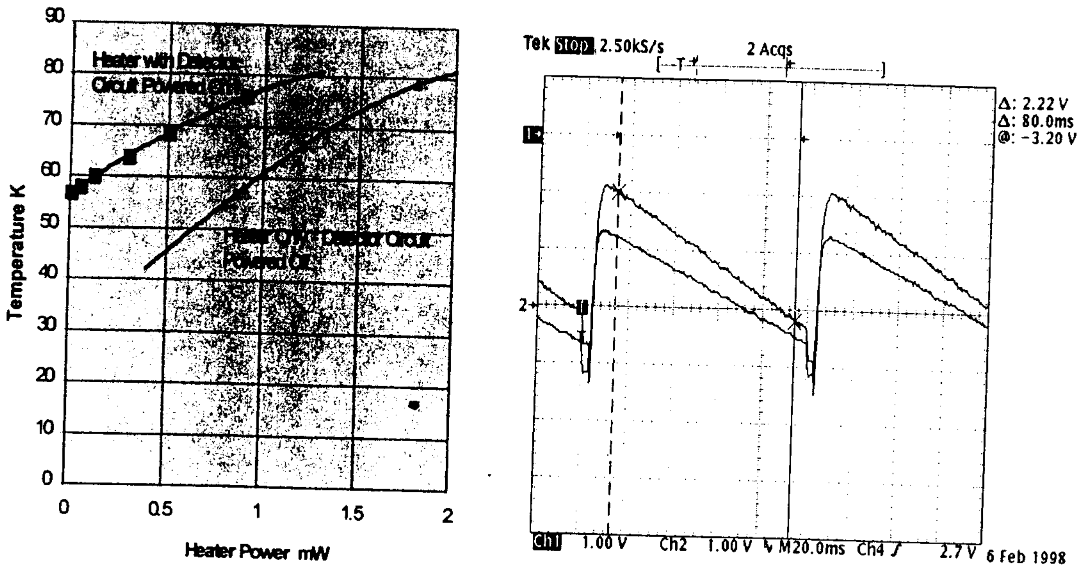


Figure 2: In a) an exploded view shows the detector circuit, platform, rigidizer for increased mechanical stability, isolator, and base. Figure 2b shows an detector circuit bonded to an isolator assembly. The multi-layer flex cable on the bottom must make a turn around the mounting post.

4. RESULTS

4.1 Thermal Isolation

First tests on a completed assembly involved measuring the thermal isolation. The base of the isolator is held at 4.2 K and the heater resistor is used to initially heat the platform. The following graph in Figure 3a contains two traces. One plot is with the heater only and one plot is the detector operating with varying heater values. The platform attains a temperature of 57 K through self-heating with only the detector circuit operating. The heater only circuit must dissipate .85 mW to achieve this temperature. By fitting



a) b)

Figure 3: In Figure 3a, the platform temperature as a function of total power dissipation is plotted. An oscilloscope trace in 3b shows an example of the output of the payload electronics. The difference in the two integration ramps corresponds to 13 fA of photocurrent.

the data and interpolating at 70 K and 80 K the detector power dissipation can be estimated to be .77 mW and .68 mW respectively. From these plots it can be determined that the platform can be operated between 57 K and 72 K using 1.5 mW or less of total power dissipation. This data was taken on an isolator with 4 legs. The current flight version with 3 legs has a smaller cross section and should give greater thermal isolation and a wider operating range. The noise characteristics of the flight units will be evaluated at a number of temperatures. A wide operating range is desirable in order to find the optimum, low noise operating point [3]. Onee an optimum operating point is determined experimentally, an active temperature control circuit in the payload electronics has the gain and resolution to maintain a platform temperature within 2 mK of the desired set point.

4.2 Photocurrent Measurements

Light incident on a photodiode produces a current into the sense node. The resulting change in the detector's drain currents (See Figure 1) is amplified in the payload electronics. The output of a differential amplifier produces a voltage across the .5 pF feedback capacitor. The resulting integration ramp is reset at a 10 Hz rate. After selecting one of 16 programmable gains, the ramp is sampled by a 16 bit A/D at 2200 Hz and a least squares line fit is made. The photocurrent can be calculated by $I = C \ dV/dt$. Noise measurements were taken with 9 fA of photocurrent as well as with no light to get the contribution from the electronics. The photon shot-noise at this level exceeded the contribution from the electronics, meeting our requirements. Additional detector measurement results on a flight quality telescope are presented in this proceeding's paper by Wang et al. Figure 3b shows an example of two integration ramps associated with significantly different light levels on each side of the dual photodiode. With a telescope scale factor of .018 fA / milli-arcsec, this 13 fA difference in light level would correspond to an angle of 722 milli-arcsec from the pointing center.

5. CONCLUSION

To date we have built 8 detector mount assemblies with circuits. Four of these have been used on the flight telescope to measure and calibrate the optics. Measurements of the electronic noise and dark current leakage verify that these units meet the science requirements. The results of vibration and centrifuge tests indicate the thermal mount is robust enough to survive launch loads. We are now in the process of building the flight units.

Acknowledgments

We are grateful to Carol Sappington at GSFC for her patience and expertise in assembly. Also greatly appreciated is the help provided by John Turneaure, Randall Kirschman, Jeff Wade, Ben Taller, Scott Fletcher, Nick Scott, Gene Tam, students Mesut Koc and Jeff Grant. This work is supported by the National Aeronautics and Space Administration, Marshall Space Flight Center, under contract NAS8-39225

References

[1] Turneaure J.P., et al., " Development of the Gravity Probe B Flight Mission", *Adv. Space Res.,* (1996).
[2] Sullivan Mark T., et al., "Detector Mount System for Thermal Isolation", *SPIE Proc.* **3132** (1997) pp 56-66.
[3] Kirschman R.K., "Transistor Noise Characteristics for Low Frequency Analog Cryogenic Instrumentation", Symposium on Low Temperature Electronics and High Temperature Superconductivity, (Electrochemical Society, INC 10 South Main St., Pennington, NJ 08534, 1993) pp 223-235.